



डा बी आर अम्बेडकर राष्ट्रीय प्रौद्योगिकी संस्थान, जालन्धर
जी टी रोड बाई पास, जालन्धर-144008, पंजाब (भारत)
Dr B R AMBEDKAR NATIONAL INSTITUTE OF TECHNOLOGY, JALANDHAR
G T Road By Pass, Jalandhar-144008, Punjab (India)
(An Institute of National Importance)

Admission to Ph.D. (Full-Time) under Visvesvaraya Ph.D. Scheme Phase –II

Applications are invited for admission to Ph.D. (Full-Time) Programme under Visvesvaraya Ph.D. Scheme Phase-II. The Broad areas of Research, Eligibility Criteria, Selection Procedure, Teaching Assistantship-cum-Scholarships etc. are given in this advertisement.

How to apply: The link to fill the online application form can be accessed through Institute website www.nitj.ac.in. An application fee of Rs.1000/- (Rs.500/- for SC/ST/PWD candidates) is required to be paid online. The candidates are required to apply online and there is no requirement to send the Hard Copy of the application form to the Institute. Application fee shall not be refunded in any case.

Last date for submission of online application form is 14/04/2024.

For more details, the candidates are advised to visit the Institute website www.nitj.ac.in for updates. All updates regarding this Advertisement will be updated on the Institute website only. All candidates are advised to visit the Institute website regularly.



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A) Broad Areas of Research

Sr. No.	Department Email address of HOD	(Broad Areas of Research)	Number of Seats
1.	Information Technology	Artificial Intelligence, Blockchain, Quantum Computing	02
2.	ECE	VLSI Design, Semi Conductor, Material Technology, Artificial Intelligence, Circuits Design and Fabrication	03
3.	Under Project	(Only Under C2S Project: Design and development of system on chip based next generation IoT system for industry 4.0 with functional safety and security features.)	02

The above seats (Sr. No. 1 and 2) may to shift the both branches in case of non-availability of the suitable candidates.

B) Eligibility Criteria

The general eligibility criteria for the minimum educational qualification will be as under:

- Master's Degree in Engineering/Technology in the relevant area of research along with Bachelor's Degree in appropriate branch of Engineering/Technology with a first class or minimum 60% marks (or CGPA of 6.5 on 10-point scale) in the qualifying examination. **GATE is mandatory.**
- Direct Ph.D. admission is also available in case of candidate with B Tech/B.E./BS (4 year) with a CGPA of 8.5 and above on a 10-point scale or 80% aggregate from a Centrally Funded Technical Institute (CFTI). All such candidates must be GATE qualified. Number of credit courses to be cleared will be 24 credits before comprehensive examination.
- **Department Specific (Information Technology):**
 - (i) Master's degree in Engineering/Technology in the relevant area of research with minimum CGPA of 6.5 on a 10-point scale or equivalent in the qualifying examination. The candidates having B. Tech degree in other than CSE/IT must be GATE qualified in CS/IT/Data Science and Artificial Intelligence discipline.
 - (ii) Bachelor's degree in Engineering/Technology from a Centrally Funding Technical Institutes (CFTI) with minimum CGPA of 8.5 or above on a 10-point scale or equivalent in the qualifying examination. In such cases, the candidates have to fulfil the requirement of minimum of 24 credits of course work.
 - (iii) MCA with M.Tech. (relevant branch) having minimum CGPA of 6.5 on a 10-point scale having GATE qualified in CS/IT/Data Science and Artificial Intelligence discipline.

OR

- (iv) The candidates should have valid JRF(UGC/CSIR) or valid GATE score (CS/IT) and satisfy any one of the following criteria:
 - a. M.Sc. (CS/IT) with M. Tech (relevant branch) research with minimum CGPA of 6.5 on a 10-point scale or equivalent in the qualifying examination.

- b. M.C.A. from CFTI/Top 100 NIRF Institutes in last 2 years with minimum CGPA of 8.5 or above on a 10-point scale or equivalent in the qualifying examination. In such cases, the candidates have to fulfill the requirement of minimum of 24 credits of course work.

C) Details of Visvesvaraya Ph.D. Scheme Phase –II:

1. Full-Time Ph.D. seats are available under the Visvesvaraya Ph.D. Scheme Phase –II funded by Ministry of Electronics and IT (MeitY) in the Department of Electronics & Communication Engineering, Information Technology and C2S Project. The details are as under:

Title of the Project		Visvesvaraya Ph.D. Scheme Phase –II, Round -II		
Funding Agency		Ministry of Electronics and IT (MeitY).		
Sr. No.	Number of Ph.D. seats	Total Seats Name of Branch	Name of Eligible Faculty	Area
1.	03	Electronics and Communication Engineering	Dr Binod Kumar Kanaujia	Circuits Design and Fabrication, AI
			Prof. B S Saini	Artificial Intelligence
			Dr Ramesh K Sunkaria	Artificial Intelligence
			Dr Ashish Raman	VLSI, Semiconductor , Circuits Design and Fabrication, AI
			Dr Asutosh Kar	Artificial Intelligence, Circuits Design and Fabrication
			Dr Balwinder Raj	VLSI Design, Semiconductor
			Dr Deepti Kakkar	Artificial Intelligence
			Dr Indu Saini	AI, VLSI
			Dr Neetu Sood	Artificial Intelligence
			Dr Manjeet Singh	Artificial Intelligence
			Dr Pawan K Verma	Artificial Intelligence
			Dr Sateesh K Awasthi	Artificial Intelligence
			Dr Sukwinder Singh	Circuit Design and Fabrication
			Dr Tarun Chaudhary	VLSI Design
			Dr Aijaz M Zaidi	Circuit Design and Fabrication
Dr Rohit Singh	AI, Circuit Design and Fabrication			
Dr Bodile Roshan	AI, Circuit Design and Fabrication			
2.	02	Information Technology	Dr Vijay Kumar	AI, BlockChain
			Dr Mohit Kumar	AI, Quantam Computing
			Dr Nisha Chaurasia	AI, Quantam Computing
			Dr Kusum Bharti	AI, Quantam Computing
			Dr. Naveen Kumar Gupta	AI, BlockChain, Quantam Computing
			Dr. Neeraj Kumar	AI, Quantam Computing
			Dr Avani Vyas	AI, Quantam Computing
			Dr. Jaspal Kaur	AI, Quantam Computing, Blockchain
			Dr. Simarjeet Singh	AI, Quantam Computing, Blockchain
3.	02 (Reserved only Under C2S Project)	ECE Department (Only Under C2S Project: Design and development of system on chip based next generation IoT system for industry 4.0 with functional safety and security features.)	Dr Ashish Raman	VLSI Design

The above Sr. No. (1 and 2) seats may shift the both branches in case of non availability of the suitable candidates.		
Position	Ph.D. fellowship	
Fellowship Amount and other Benefits	Fellowship	Rs. 38750/- (1 st and 2 nd year) Rs. 43750/- (3 rd , 4 th and 5 th year)
	Reimbursement of Rent	As per Funding Agency Norms
	Research Contingency grant	Rs. 1,20,000/ year
	Other/detailed Terms and Conditions: As per Visvesvaraya Ph.D. Scheme Phase – II, Round - II funded by Ministry of Electronics and IT (MeitY). Link : https://Ph.D..digitalindiaincorporation.in/home	
Eligibility Criteria and Admission Procedure	As per the Ph.D. Full-Time (under Institute Fellowship)	
Broad Areas of Research	ECE: ESDM: VLSI Design, Semi Conductor, Material Technology, Artificial Intelligence, Circuits Design and Fabrication, Antenna Design for Biomedical Applications	
	Information Technology : Blockchain, Quantum Computing	
Nodal Officer/PI/Contact Person	Dr Ashish Raman (ECE Department) Email: ramana@nitj.ac.in	

D) Admission Procedure

- i. Shortlisting of the candidates will be on GATE score. Mere shortlisting of an applicant does not confirm admission to Ph.D. Programme. The admission shall be solely based upon the performance of individuals during “presentation and interaction” and availability of the Supervisor in the proposed area of research.
- ii. The Department Admission Committee for the Departments shall recommend the suitable candidates for admission based on its assessment of presentation and interaction.
- iii. The Department Admission Committee/Institute reserves the right not to recommend any candidate for admission to Ph.D. in the respective Department if the performance of the shortlisted candidates is not found satisfactory during “presentation and interaction”. The decision of Department Admission Committee (approved by the competent authority of the Institute) shall be final.
- iv. The merit list of the selected candidates (based on presentation & interaction) shall be prepared on marks basis. A candidate who scores less than 40 marks (out of 100) for “presentation & interaction” shall not be considered “qualified” for admission to Ph.D. programme and his/her name shall not be recommended for admission by Departmental Admission Committee.
- v. The list of recommended candidates for admission to Ph.D. (Full-Time) programme shall be made in order of merit.
- vi. All the admitted candidates shall be governed by the Ph.D. regulations of the Institute, guidelines of the Visvesvaraya Ph.D. Scheme Phase –II funded by Ministry of Electronics and IT (MeitY) and other instructions issued by the Institute time to time as well as the Ministry of Electronics and IT (MeitY).

E) Other Issues

- i. Category (UR/EWS/OBC/SC/ST/PWD) once chosen by the applicant in his/her application form shall not be changed at a later stage. The candidate (s) applying under (EWS/OBC/SC/ST/PWD) category shall have to produce a valid category certificate issued by the competent authority.

- ii. OBC-NCL/EWS Certificate must have been issued on or after **1st April, 2023** so that the candidates from creamy layer are identified. No certificate issued before this date shall be acceptable.
- iii. All the candidates should ensure that they possess the required educational qualification by the last date of submission of the application under this Advertisement.
- iv. **Certificate Checking:** The certificates (in original) of all the candidates recommended for admission shall be checked by the individual Department before deposition of fee by the candidates.
- v. The candidate (in service) applying for full-time Ph.D. programmes need to apply through proper channel. Any application without “No Objection Certificate” from the employer shall not be considered for shortlisting.
- vi. The application without proof of application fee as applicable/self-attested copies of documents/certificates/testimonials shall be rejected and shall not be considered for shortlisting.
- vii. The syllabus of the Institute Level Screening Test will be that of GATE examination and the Screening Test will be in MCQ mode.

F) Fellowship

The candidates admitted under this Advertisement will be eligible for fellowship as mentioned in the Table at **C)** above. Fellowship shall be paid as per the guidelines of the Visvesvaraya Ph.D. Scheme Phase –II funded by Ministry of Electronics and IT (MeitY) and other instructions issued by the Ministry of Electronics and IT (MeitY) in this regard. The period of the project is 05 years or till the completion of the project whichever is earlier. Fellowship will be started from the date of joining by the candidate in the Department and fellowship will be paid for a maximum duration of 05 Years or till the completion of project whichever is earlier (as per project guidelines).

H) Important Dates

Sr. No.	Activity	Date
1.	Last date for submission of Applications	14/04/2024
2.	Display of list of candidates eligible for presentation & interaction	15/04/2024
4.	Presentation/interaction by all eligible candidates	19/04/2024
5.	Display of list of selected candidates	19/04/2024 (5.00 PM)
6.	Deposition of fee & Registration	22/04/2024
7.	Commencement of classes	Will be notified separately by the Department
8.	Last date of fee submission & Registration	26/04/2024

All the dates mentioned above are tentative subject to change at any stage by the competent authority. All the candidates interested in seeking admission are requested to visit the Institute website regularly for updates.

- I) All disputes pertaining to the admissions shall fall within the jurisdiction of Jalandhar only.
- J) All admissions will be provisional till these are confirmed subject to medical fitness, payment of all the fees, fulfillment of eligibility conditions, and verifications of certificates by the Academic Section of the Institute.
- K) After payment of fee (application/admission fee), no fee refund request shall be entertained in any case.
- L) The Institute reserves the right to modify or cancel this Advertisement/any part of this Advertisement at any stage.
- M) It is mandatory for all applicants to fill the preferences of prospective supervisors on the below mentioned link by 14.04.2024:

Link :

- N)** The list of the Faculties are available in the **Annexure-I**. Further, the candidates can view the research domain of the Faculties by visiting the Department Website from the Academics Menu of the Institute Website.

**-Sd/-
Dean Academic**

Annexure-I

Electronics and Communication Engineering Department		
Name Of Faculty	Working	Emerging Area
Dr Binod Kumar Kanaujia	ESDM	Circuits Design and Fabrication
Dr Ramesh K Sunkaria	ESDM	Artificial Intelligence
Dr Ashish Raman	ESDM	VLSI, Semiconductor , Circuits Design and Fabrication,
Prof. B S Saini	ESDM	Artificial Intelligence
Dr Asutosh Kar	ESDM	Artificial Intelligence, Circuits Design and Fabrication
Dr Balwinder Raj	ESDM	VLSI Design, Semiconductor
Dr Deepti Kakkar	ESDM	Artificial Intelligence
Dr Indu Saini	ESDM	AI, VLSI
Dr Neetu Sood	ESDM	Artificial Intelligence
Dr Manjeet Singh	ESDM	Artificial Intelligence
Dr Pawan K Verma	ESDM	Artificial Intelligence
Dr Sateesh K Awasthi	ESDM	Artificial Intelligence
Dr Sukwinder Singh	ESDM	Circuit Design and Fabrication
Dr Tarun Chaudhary	ESDM	VLSI Design
Dr Rohit Singh	ESDM	AI, Circuit Design and Fabrication
Dr Aijaz M Zaidi	ESDM	Circuit Design and Fabrication
Dr Bodile Roshan	ESDM	AI, Circuit Design and Fabrication
Information Technology Department Information Technology Department		
Dr Vijay Kumar	ITES	AI, Block Chain
Dr Mohit Kumar	ITES	AI, Quantam Computing
Dr Nisha Chaurasia	ITES	AI, Quantam Computing
Dr Kusum Bharti	ITES	AI, Quantam Computing
Dr. Naveen Kumar Gupta	ITES ITES	AI, Quantam Computing, Blockchain AI, BlockChain, Quantam Computing
Dr. Neeraj Kumar	ITES	AI, Quantam Computing
Dr Avani Vyas	ITES	AI, Quantam Computing
Dr. Jaspal Kaur	ITES	AI, Quantam Computing, Blockchain
Dr. Simarjeet Singh	ITES	AI, Quantam Computing, Blockchain
ECE Department (Reserve only Under C2S Project: Design and development of system on chip based next generation IoT system for industry 4.0 with functional safety and security features.)		
Dr Ashish Raman	ESDM	VLSI, Semiconductor , Circuits Design and Fabrication, AI