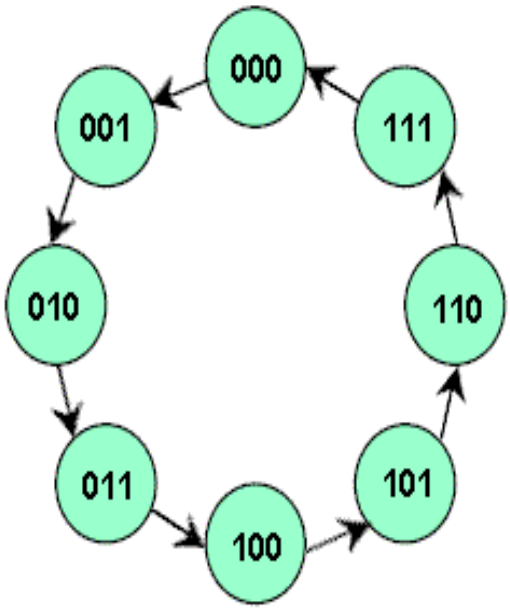
Digital Electronics

Synchronous Counters

In a *synchronous counter*, also known as a *parallel counter*, all the flip-flops in the counter change state at the same time in synchronism with the input clock signal. The clock signal in this case is simultaneously applied to the clock inputs of all the flip-flops. The delay involved in this case is equal to the propagation delay of one flip-flop only, irrespective of the number of flip-flops used to construct the counter. In other words, the delay is independent of the size of the counter. Since the different flip-flops in a synchronous counter are clocked at the same time, there needs to be additional logic circuitry to ensure that the various flip-flops toggle at the right time. Using parallel counters, any binary or non-binary sequences can be obtained by using the design procedure.

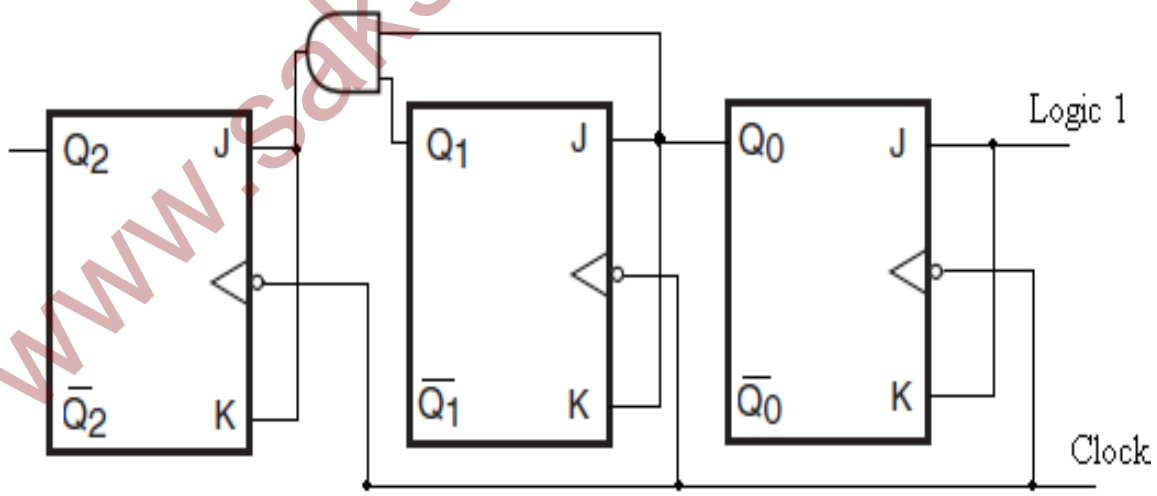
MOD 8 Counter:

To obtain MOD 8 parallel counter, 3 flip-flops are required. Clock input will be common for all flip-flops and hence the flip-flops should not be in toggle mode always and additional hardware is required to obtain the sequence. The state diagram and table for the required counter is as shown below.



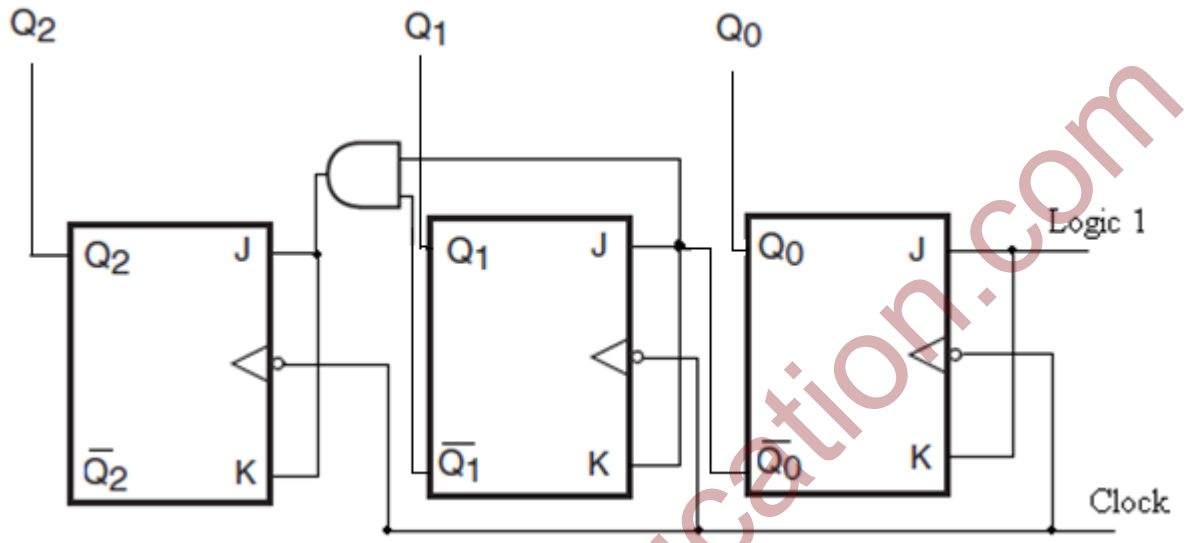
Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

In the given count sequence, we find that flip-flop FF0 toggles with every clock pulse, flip-flop FF1 toggles only when the output of FF0, Q_0 is in the '1' state, flip-flop FF2 toggles only with those clock pulses when the outputs of FF0 and FF1 are both in the logic '1' state. Such logic can be easily implemented with AND gates.



MOD 8 DOWN Counter:

The circuit diagram for DOWN counter is as shown below where Q_0' *and* Q_1' are given to the inputs of flip-flop directly (or using AND gate).



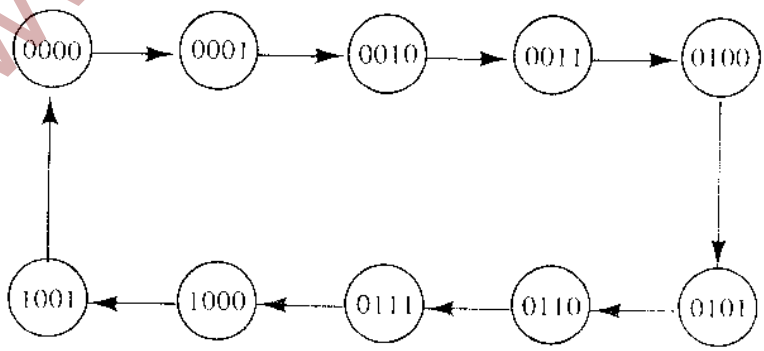
Examples:

1. Design a BCD counter using JK flip-flops.

Sol:

To design a BCD counter or decade counter or MOD 10 counter, 4 flip-flops are required.

State diagram:



State table:

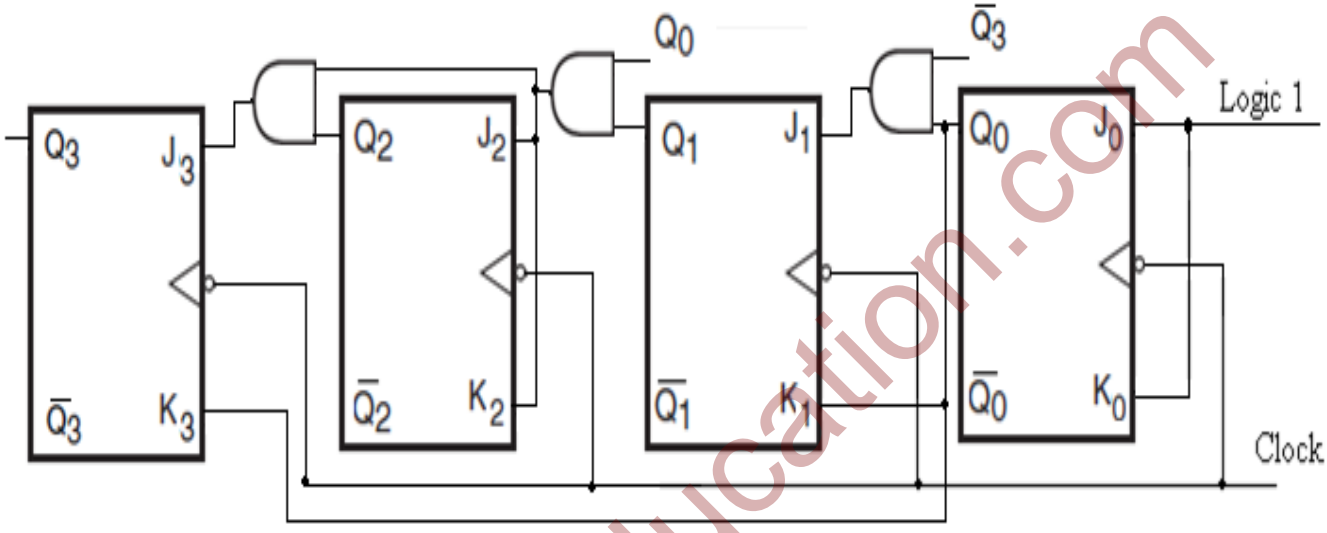
Present State (PS)				Next State (NS)			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

Circuit excitation and output table:

Present State (PS)				Next State (NS)				Flip-flop Input functions							
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

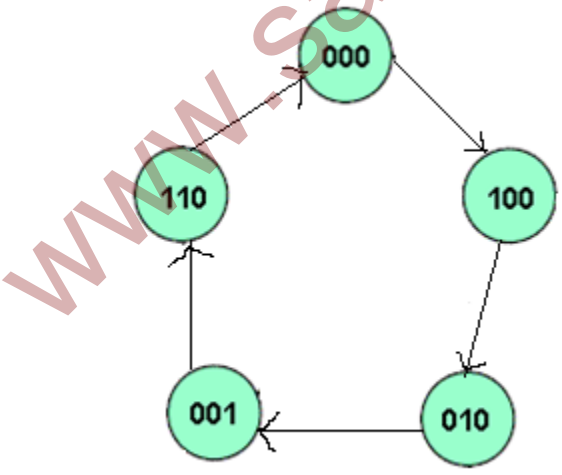
By using K-maps, we get expressions for the flip-flop input functions.

$J_0 = K_0 = 1\,; J_1 = Q_3' Q_0\,, K_1 = Q_0\,; J_2 = K_2 = Q_1 Q_0\,; J_3 = Q_2 Q_1 Q_0\,, K_3 = Q_0$



2. Design a counter using JK flip-flops for the following binary sequence: 0, 4, 2, 1, 6 and repeat.

Sol:



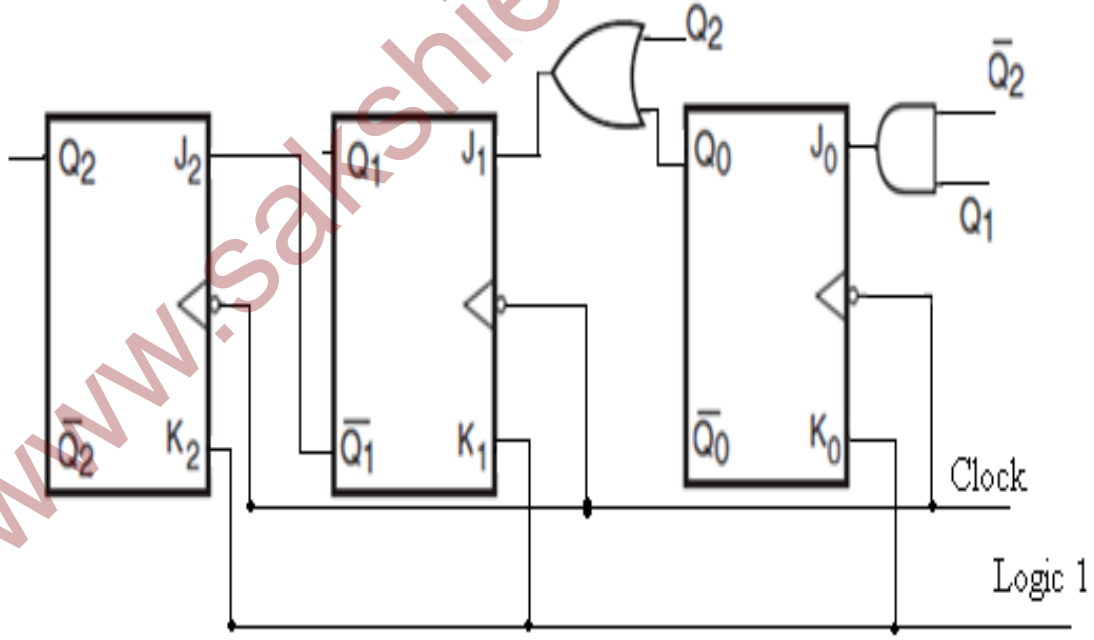
Present State (PS)			Next State (NS)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0
0	0	1	1	1	0
0	1	0	0	0	1
1	0	0	0	1	0
1	1	0	0	0	0

Circuit Excitation and output table:

Present State (PS)			Next State (NS)			Flip-flop Input functions					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	1	0	0	1	X	0	X	0	X
0	0	1	1	1	0	1	X	1	X	X	1
0	1	0	0	0	1	0	X	X	1	1	X
1	0	0	0	1	0	X	1	1	X	0	X
1	1	0	0	0	0	X	1	X	1	0	X

By using K-maps, we get.

$J_0 = Q_2'Q_1$, $K_0 = 1$; $J_1 = Q_2 + Q_0$, $K_1 = 1$; $J_2 = Q_1'$, $K_2 = 1$;



Lockout:

The counter just discussed utilizes only five out the total number of eight states available in a counter having three flip-flops. The counter may enter one of the unused states and may keep moving between the unused states and not come out of this situation. This condition may develop because of external noise, which may affect states of the flip-flops. If a counter has unused states with this characteristic, it is said to suffer from lockout. The lockout situation can be avoided by so arranging the circuit that whenever the counter happens to be in an unused state, it reverts to one of the used states. The above circuit can be designed to avoid lock out by making the next states of unused states (3, 5, 7) to any valid state. Hence to avoid lockout or to make the counter self-starting, the next state of any invalid state must be a valid initial state.

The advantages of parallel counter are its speed of operation and any type of sequence can be obtained. The drawback is its hardware part where we require additional gates along with required number of flip-flops.