Digital Electronics

Sequence Detector

A sequence detector is a sequential logic circuit which accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected. There are two basic types of detectors: overlap and non-overlap. In a sequence detector that allows overlap, the final bits of one sequence can be the start of another sequence.

In the design of sequence detector, the state diagram is important and must be obtained initially. Using the state diagram, the procedure is similar to the design procedure of sequential circuits.

To obtain the state diagram the following rules are followed:

1. Identify the number of states in which the circuit will move by looking at the number of bits in the sequence. For example, to detect a sequence of length 4 bits, 4 states will be observed.
2. The circuit will move to the next state only if desired bit is received. If not, the circuit remains in the same state or it moves back to the any one of the previous states.
3. By observing the received input bits, the next state of the circuit is identified.

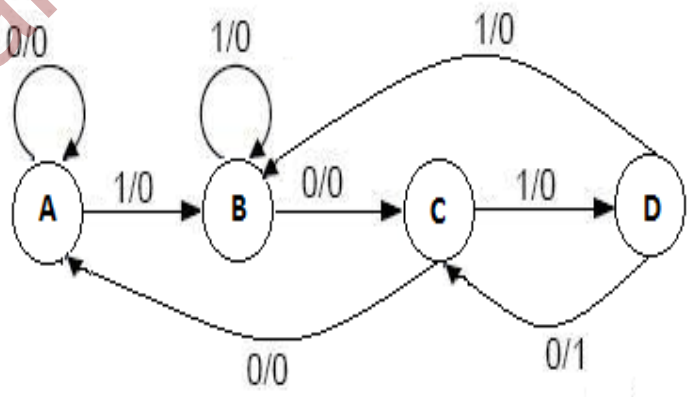
D flip-flops will be used for the design of sequence detectors.

Examples:

1. Design a sequence detector to detect a sequence 1010. Overlapping of sequences is permitted.

Sol: Since the number of bits is 4, four states can be used. The circuit consists of one input and one output. The output will be 1 whenever the sequence is detected.

If the first bit received is 0, the circuit remains in the same state A as it is not the required bit. If the bit is 1, the circuit goes to next state B. If the second bit is 0, circuit goes to next state C and remains in the same state B if the bit is 1. Since overlapping is permitted, this 1 can be used to start the sequence. If the third bit is 0, as it is not useful in any way, the next state should be A. If it is 1, the next state is D. If the fourth bit is 0, the sequence is completed and the next state should be C as previous 10 can be used for the next sequence. The output will become 1 when sequence is detected and is equal to 0 in all other cases. If the fourth bit received is 1, the next state must be B to start the next sequence.



State Table:

Present State (PS)	Next State (NS)		Output (F)	
	$p = 0$	$p = 1$	$p = 0$	$p = 1$
A	A	B	0	0
B	C	B	0	0
C	A	D	0	0
D	C	B	1	0

Let A = 00, B = 01, C = 10, and D = 11

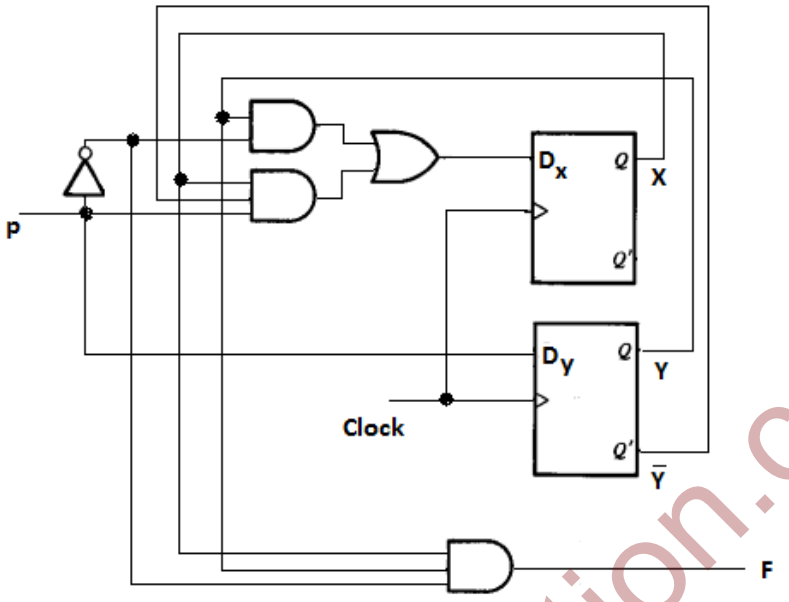
Circuit excitation and Output table:

Present State		Input	Next State		Flip-flop Input functions		Output
X	Y	p	X	Y	D_X	D_Y	F
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0
1	0	0	0	0	0	0	0
1	0	1	1	1	1	1	0
1	1	0	1	0	1	0	1
1	1	1	0	1	0	1	0

After simplification, the final expressions are

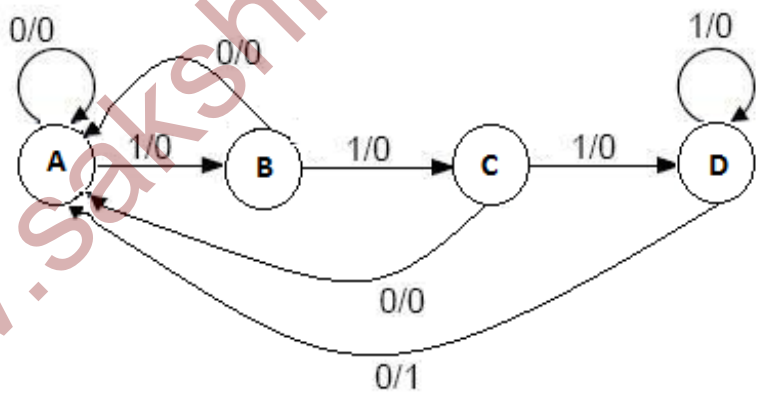
$$D_X = Yp' + XY'p;\ \ D_Y = p;\ F = XYp'$$

The circuit diagram can be obtained by implementing these expressions.



2. Design a sequence detector to detect a sequence 1110. Overlapping of sequences is permitted.

Sol:



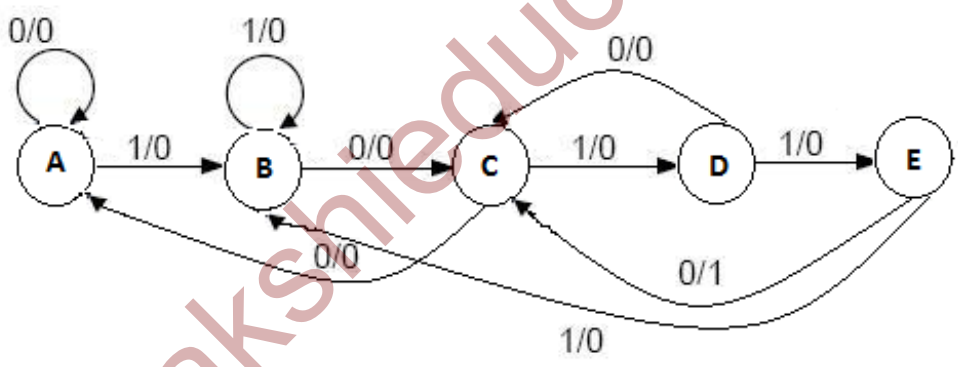
If the first bit received is 0, the circuit remains in the same state A as it is not the required bit. If the bit is 1, the circuit goes to next state B. If the second bit is 0, circuit goes to previous state A and goes to the next state C if the bit is 1. If the third bit is 0, as it is not useful in any way, the next state should be A. If it is 1, the next state is D. If the fourth bit is 0, the sequence is completed and the next state should be A as the sequence must be started again. The output will

become 1 when sequence is detected and is equal to 0 in all other cases. If the fourth bit received is 1, the next state must be D to complete the next sequence after receiving 0 bit.

Using the above example procedure, we design the circuit.

3. Design a sequence detector to detect a sequence 10110. Overlapping of sequences is permitted.

Sol: There are 5 bits and hence 5 states are used. The following is the state diagram for the sequence detector. State reduction technique must be used to verify the reduction of states and state assignment to assign the states.



Present State (PS)	Next State (NS)		Output (F)	
	$p = 0$	$p = 1$	$p = 0$	$p = 1$
A	A	B	0	0
B	C	B	0	0
C	A	D	0	0
D	C	E	0	0
E	C	B	1	0

No two states are equivalent and hence no reduction is possible. Let

A = 000, B = 001, C = 010, D = 011, E = 100

Using these states, prepare the circuit excitation and output table and obtain the simplified expressions. Draw the logic diagram.