Digital Electronics

Registers

A flip-flop can store or remember or register a single bit of information. A flip-flop is therefore referred to as a one bit register. When an array of flip-flops has a number of bits in storage, it becomes necessary an occasion to shift bits from one flip-flop to another. An array of flip-flops which permits this shifting is called a shift register. Shift registers have found considerable application in arithmetic operations. Since moving a binary number one bit to the left is equivalent to multiplying the number by 2 and moving the number one bit position to the right amounts to dividing the number by 2. Thus, multiplications and divisions can be accomplished by shifting data bits. Shift registers find considerable application in generating a sequence of control pulses. The basic building block in all shift registers is the flip-flop, mainly a D-type flip-flop.

Shift registers can be classified into four distinct groups.

1. *Serial-in serial-out (SISO),* in which data can be moved serially in and out of the register, one bit at a time.

2. *Serial-in parallel out (SIPO),* in which the register is loaded serially, one bit at a time, and when an output is required the data stored in the register can be read in parallel form.

3. *Parallel-in serial-out (PISO),* in which all the flip-flops are loaded simultaneously and when an output is required, the data stored is removed serially from the register one bit at a time under clock control.

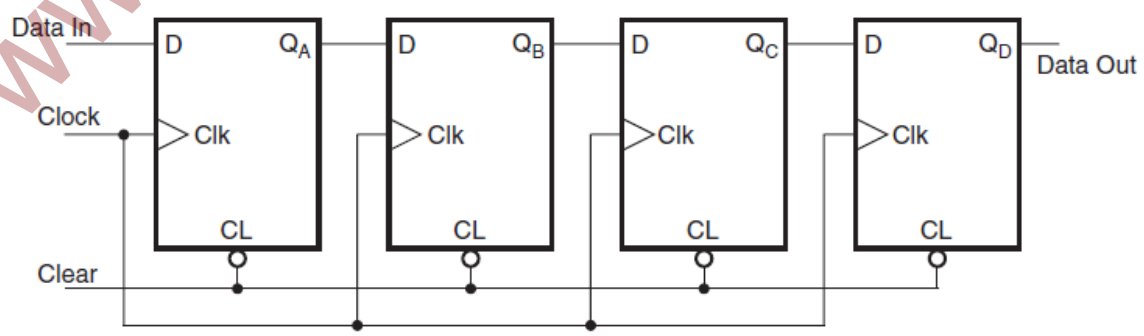
4. *Parallel-in parallel-out (PIPO),* in which all the flip-flops in the register are loaded simultaneously, and when an output is required the flip-flops are read simultaneously.

Serial-In Serial-Out Shift Register (SISO):

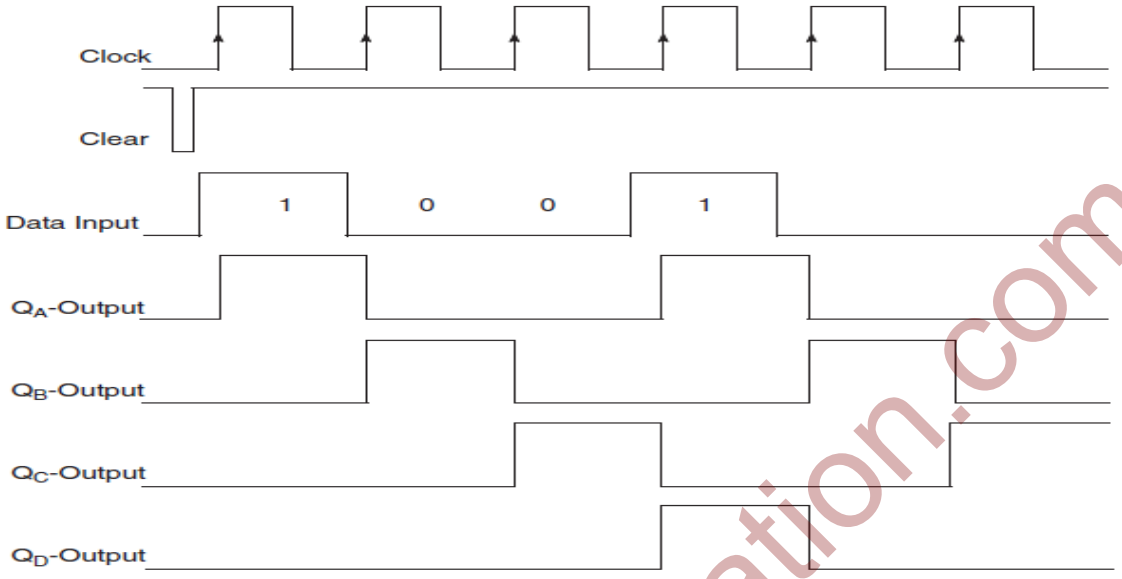
In serial – in serial – out shift register (SISO), the data in the flip-flops will shift serially from one flip-flop to another, either to left or right side.

4 bit Right Shift register:

A reset applied to the CLEAR input of all the flip-flops resets their Q outputs to 0s. During the first clock transition, the Q_A output goes from logic '0' to logic '1'. The outputs of the other three flip-flops remain in the logic '0' state as their D inputs were in the logic '0' state at the time of clock transition. During the second clock transition, the Q_A output goes from logic '1' to logic '0' and the Q_B output goes from logic '0' to logic '1', again in accordance with the logic status of the D inputs at the time of relevant clock transition. Thus, we have seen that a logic '1' that was present at the data input prior to the occurrence of the first clock transition has reached the Q_B output at the end of two clock transitions. This bit will reach the Q_D output at the end of four clock transitions. In general, in a four-bit shift register of this type a data bit present at the data input terminal at the time of the n^{th} clock transition reaches the Q_D output at the end of the $(n+4)^{th}$ clock transition. During the fifth and subsequent clock transitions, data bits continue to shift to the right and at the end of the eighth clock transition the shift register is again reset to all 0s. Thus, in a four-bit serial-in serial-out shift register, it takes four clock cycles to load the data bits and another four cycles to read the data bits out of the register.



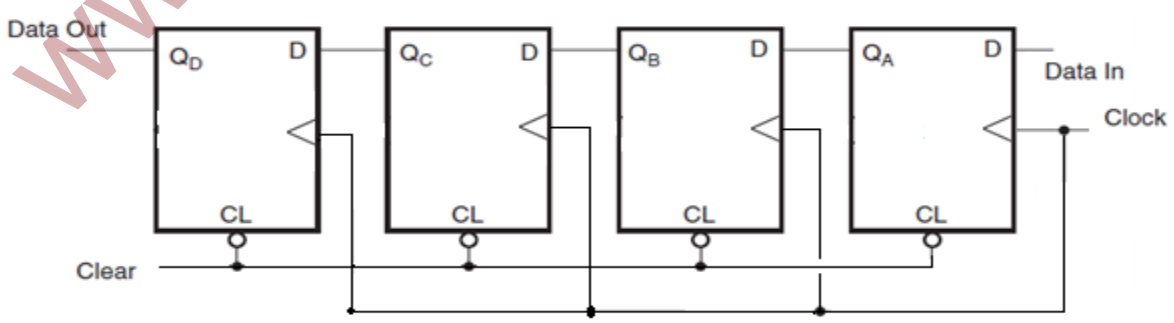
Timing waveforms:



Contents of the right shift register:

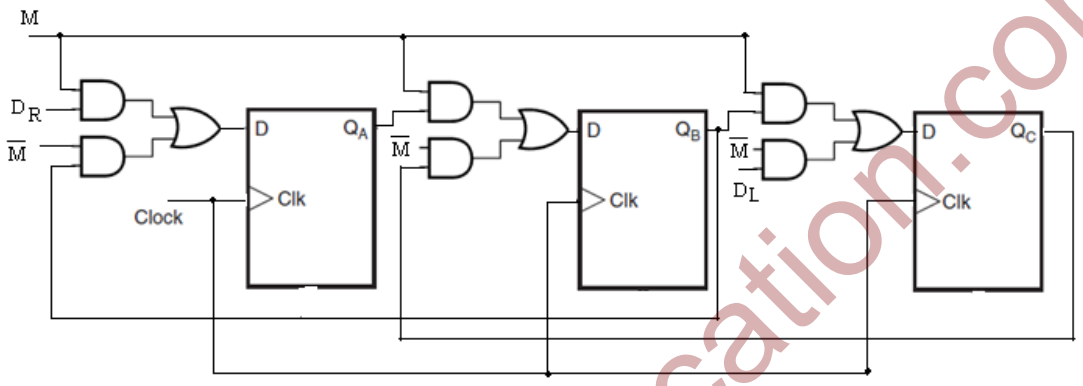
Clock	Q_A	Q_B	Q_C	Q_D
Initial contents	0	0	0	0
After first clock transition	1	0	0	0
After second clock transition	0	1	0	0
After third clock transition	0	0	1	0
After fourth clock transition	**1**	**0**	**0**	**1**
After fifth clock transition	0	1	0	0
After sixth clock transition	0	0	1	0
After seventh clock transition	0	0	0	1
After eighth clock transition	**0**	**0**	**0**	**0**

4 bit Left Shift Register:



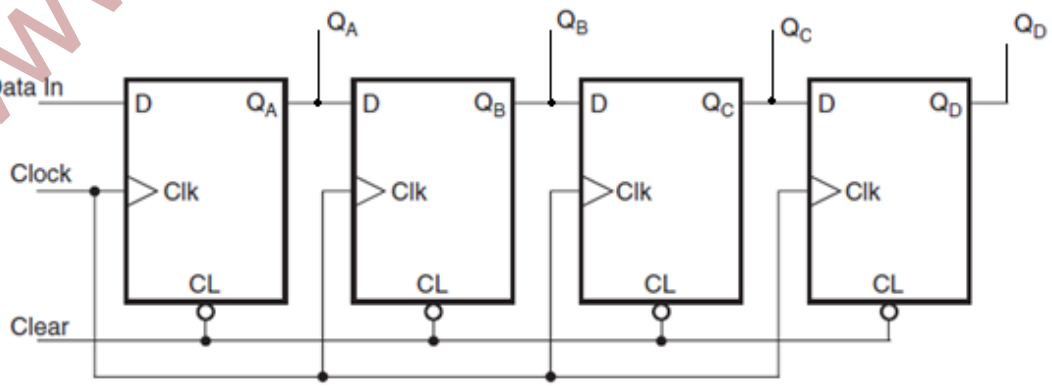
Bi-directional Shift Register or Shift Right/Shift Left Register:

A shift register with a facility to shift in either left or right direction is known as a bidirectional shift register. A mode input or control input M is used, so that when $M = 1$, right shift is performed and when $M = 0$, left shift will be performed. D_R is the data bit for right shift and D_L is the data bit for left shift.



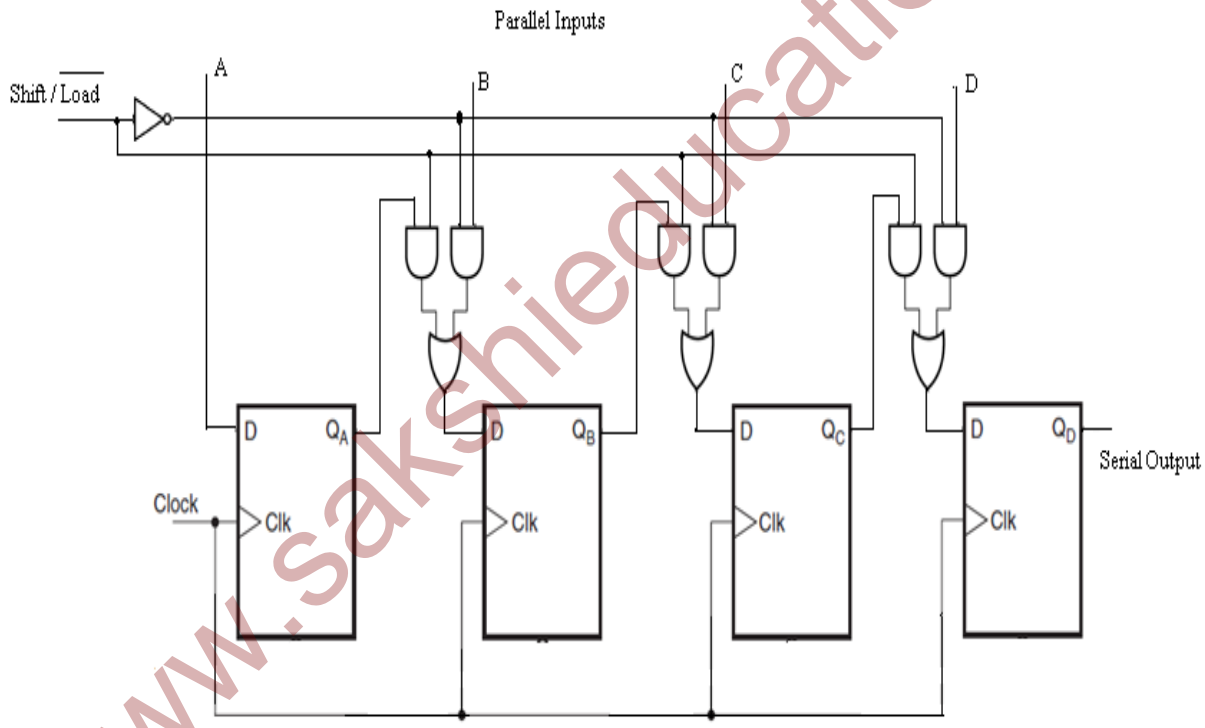
Serial-In Parallel-Out Shift Register (SIPO):

A serial-in parallel-out shift register is architecturally identical to a serial-in serial-out shift register except that in the case of SIPO, all flip-flop outputs are considered to take parallel outputs. The data will enter into the register serially through one flip-flop and after loading the contents into the flip-flops, the outputs are obtained from all flip-flops simultaneously at the same instant. It is compulsory to ensure loading before shifting the data.



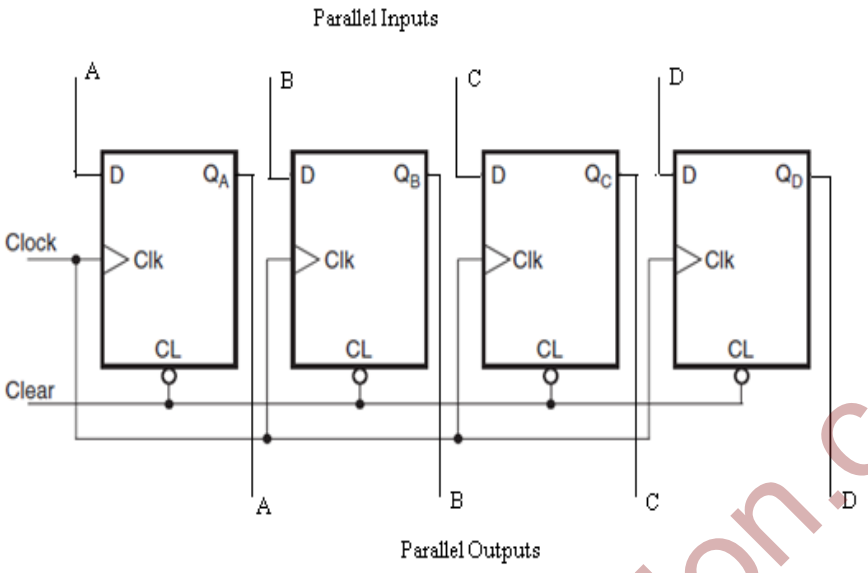
Parallel-In Serial-Out Shift Register (PISO):

In Parallel- in Serial-out shift register, the data will be loaded into the shift register through all flip-flops simultaneously and the output will be taken from the last flip-flop. Before the data is shifted serially, data should be loaded into the flip-flops and this is performed using a control input $hift/\overline{Load}$. When the mode input is logic 0, the AND gates associated with the inputs will be in working state, and hence the inputs will be loaded in to the flip-flops. After ensuring loading, the control input is changed to logic 1 and shifting operation will be initiated as the AND gates associated with the flip-flop's outputs are in working condition.



Parallel-In Parallel-Out Shift Register:

For parallel in-parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The number of clock pulses required to complete the shifting is only one.



Universal Shift Register:

A universal shift register can be made to function as any of the four types of register discussed in previous sections. That is, it has serial/parallel data input and output capability, which means that it can function as serial-in serial-out, serial-in parallel-out, parallel-in serial out and parallel-in parallel-out shift registers. A 4 bit Universal shift register consists of four D flip-flops and four multiplexers each one with one flip-flop. By controlling the select inputs, the required shifting can be obtained.