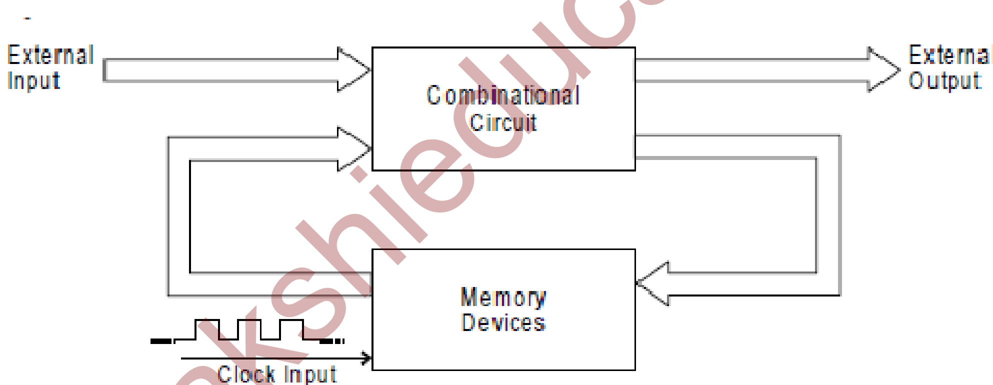
Sequential Logic Functions

Digital logic circuits can be classified as either combinational or sequential circuits. A combinational circuit is one where the output at any time depends only on the present combination of inputs at that point of time with total disregard to the past state of the inputs. The other category of logic circuits, called sequential logic circuits, comprises both logic gates and memory elements such as flip-flops. Owing to the presence of memory elements, the output in a sequential circuit depends upon not only the present but also the past state of inputs.



A block diagram of a sequential circuit is shown in the figure. A feedback path is formed by using memory elements, input to which is the output of combinational circuit. The binary information stored in memory element at any given time is defined as the state of sequential circuit at that time. Present contents of memory elements is referred as the present state.

The combinational circuit receives the signals from external input and from the memory output and determines the external output. They also determine the condition and binary values to change the state of memory. The new contents of the memory elements are referred as next state and depend upon the external input and present state. Hence a sequential circuit can be completely specified by a time sequence of inputs, outputs and the internal states. In general, clock is used to control the operation. The clock frequency determines the speed of operation of a sequential circuit.

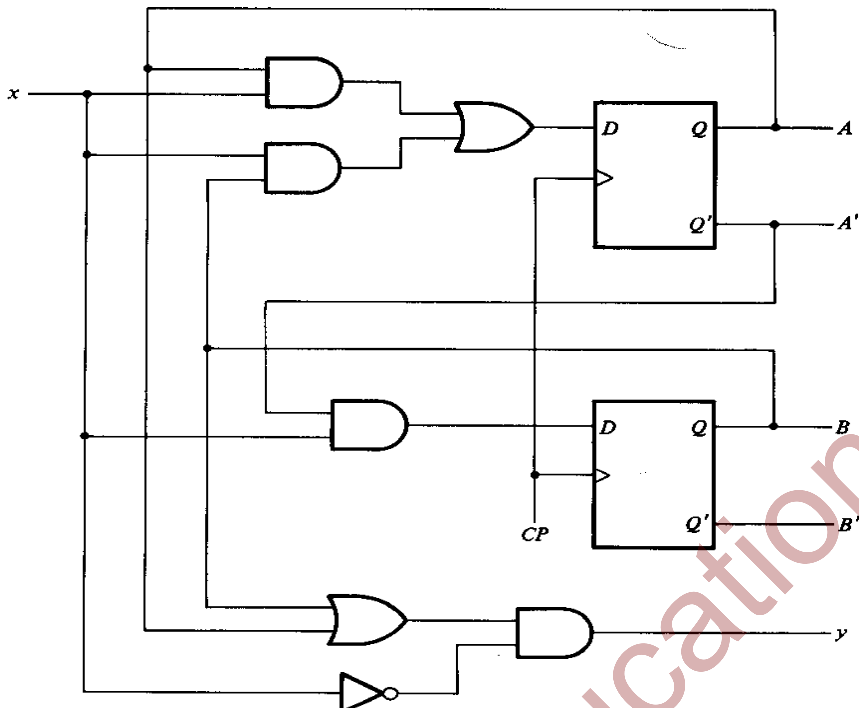
There are two types of sequential circuits, namely synchronous and asynchronous sequential circuits. Sequential circuits, whose behavior depends upon the sequence in which the inputs are applied, are called Asynchronous Sequential Circuits. In these circuits, the outputs are affected at any time by simply changing the inputs. Memory elements used in asynchronous circuits mostly are time delay devices. The memory capability of time delay devices is due to the propagation delay of the devices. Propagation delay produced by the logic gates is sufficient for this purpose. Hence "An Synchronous sequential circuit can be regarded as a combinational circuit with feedback". However feedback among logic gates makes the asynchronous sequential circuits, often susceptible to instability. As a result they may become unstable. This makes the design of asynchronous circuits very tedious and difficult.

A Synchronous Sequential Circuit may be defined as a sequential circuit, whose state can be affected only at the discrete instants of time. The synchronization is achieved by using a timing device, termed as System Clock Generator, which generates a periodic train of clock pulses. A synchronous sequential circuit that uses clock at the input of memory elements are referred as Clocked Sequential circuit.

Analysis of Sequential Logic Circuits:

The behavior of a sequential circuit is determined from the inputs, the outputs, and the state of its flip-flops. The outputs and the next state sre both a function of the inputs and the present state. The analysis of a sequential circuit consists of obtaining a table or a diagram for the time sequence of inputs, outputs, and internal states.

Example:



The above circuit consists of two D flip-flops A and B, an input x, and an output y.

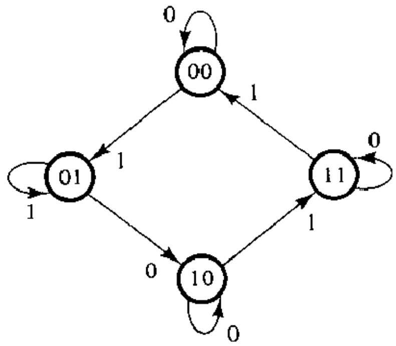
Design of Sequential Circuits:

Design Procedure:

1. The word description of the circuit behavior is stated.
2. From the given information about the circuit, obtain the state table.
3. Using state reduction techniques, number of states may be reduced.
4. Assign binary values to each state if the state table obtained in step 2 or 3 contains letter symbols.
5. Determine the number of flip-flops needed and assign a letter symbol to each.
6. Choose the type of flip-flop to be used.
7. From the state table, derive the circuit excitation and output tables.
8. Using the K-maps, derive the circuit output functions and the flip-flop input functions.
9. Draw the logic diagram.

Example:

Design a sequential logic circuit for the given state diagram. Use JK flip-flops.



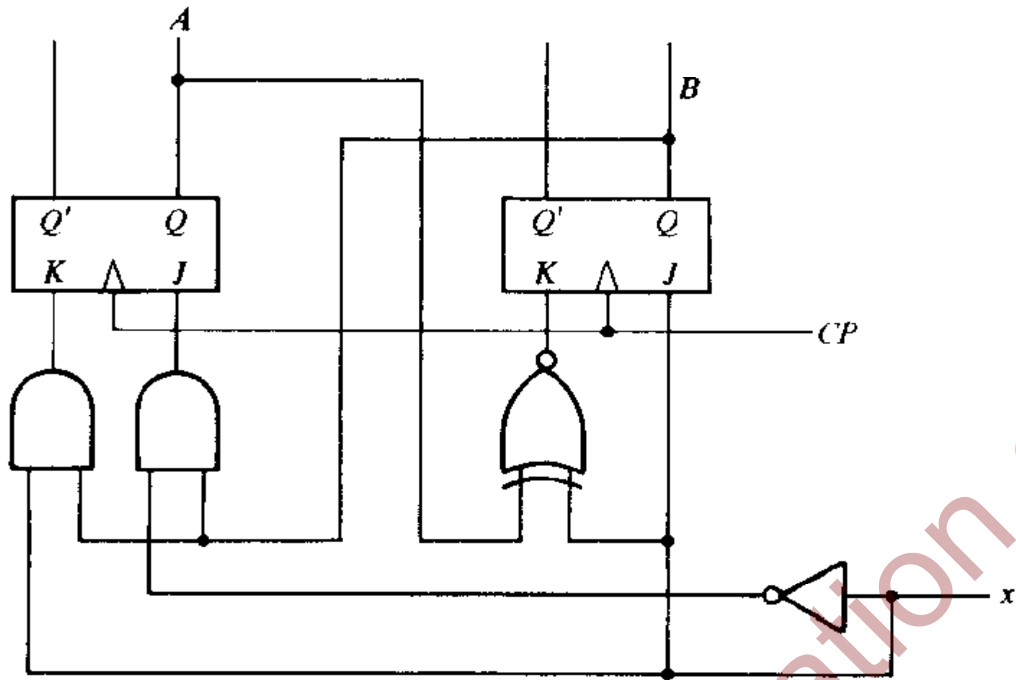
Sol:

Present State (PS)		**Next State (NS)**			
		$x = 0$		$x = 1$	
A	B	A	B	A	B
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	1	0	0

Present State		**Input**	**Next State**		**Flip-flop Input functions**			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

By using K-maps we get,

$J_A = Bx'$; $K_A = Bx$; $J_B = x$; $K_B = (A \oplus x)'$


A
B
Q'
Q
K
J
Q'
Q
K
J
CP
x