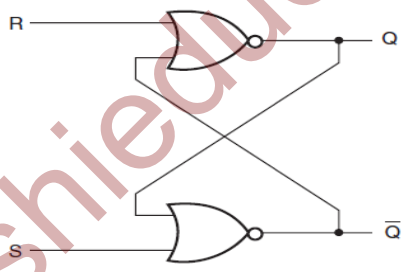
Digital Electronics

Flip-Flops

Flip-flops:

The memory elements used in sequential logic circuits are called as flip-flops. A flip-flop is a 1-bit memory element or a cell which is capable of storing 1-bit of information. It has two stable states, 1-state or set state and 0-state or reset state. It is also known as Bi-stable multi-vibrator or Eccles-Jordan circuit. A flip-flop consists of two outputs, normal output Q and complemented output Q'.

RS Latch using NOR gates:

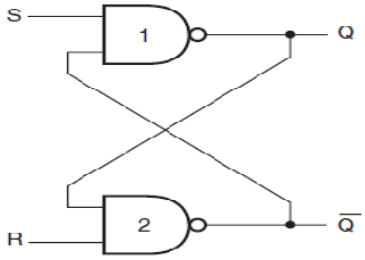


Truth table:

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Indeterminate State

SR latch using NAND gates:



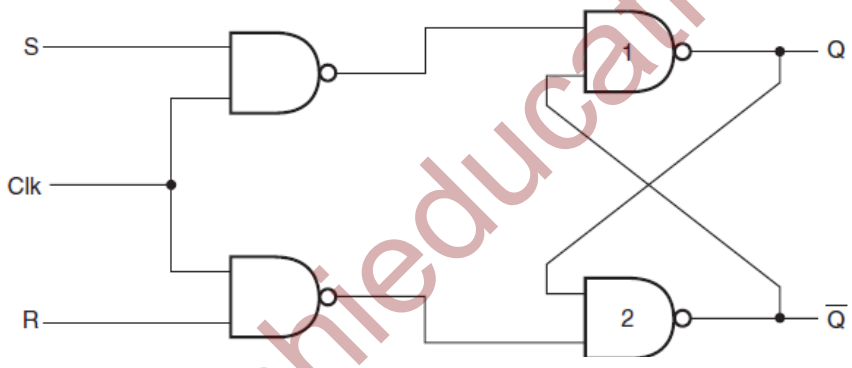
Truth table:

S	R	Q	Q'
0	1	1	0
1	1	1	0
1	0	0	1
1	1	0	1
0	0	1	1

S	R	Q_{n+1}
0	0	Indeterminate State
0	1	1
1	0	0
1	1	Q_n

Clocked SR Flip-flop:

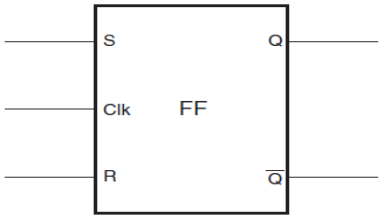
The basic flip-flop circuit or NAND latch can be modified as shown and it is known as SR flip-flop.



With clock input LOW, irrespective of S and R, the output will remain same as the previous state. The flip-flop will not respond to the inputs until clock is LOW. With clock input HIGH, the flip-flop will work normally and responds the inputs.

The operation of the flip-flop can be explained with the help of characteristic table and characteristic equation. A characteristic table completely specifies the logic behavior of a flip-flop. The next state of the flip-flop is expressed as a function of present state and inputs.

Logic Symbol:



Characteristic Table:

Q	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

Characteristic Equation:

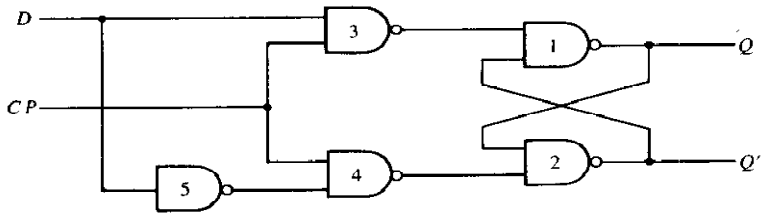
$$Q_{n+1} = S + R'Q_n$$

Truth table:

Clk	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Indeterminate State

D Flip-flop:

The D flip-flop can be obtained from SR flip-flop by connecting an inverter between S and R, i.e., the D input goes directly to the S input and its complement is applied to the R input. If D is 1, the Q output goes to 1, placing the circuit in the set state. If D is 0, output Q goes to 0 and the circuit switches to the clear state. The D flip-flop receives the designation from its ability to hold data into its internal storage. This type of flip-flop is sometimes called a gated D –latch.



Truth table:

D	Q_{n+1}
0	0
1	1

Characteristic table:

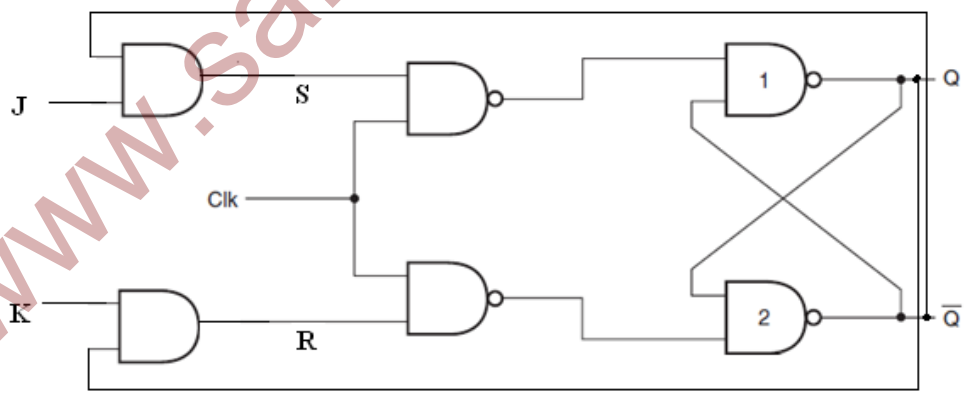
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic Equation:

$$D = Q_{n+1}$$

JK Flip-flop:

The indeterminate state in SR flip-flop can be eliminated by modifying the SR flip-flop and it is known as JK flip-flop. The input marked J is for set and the input marked K is for reset. When both inputs J and K are equal to 1, the flip-flop switches to its complement state, that is, if $Q = 1$, it switches to $Q = 0$, and vice versa.



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Truth table:

Clk	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Q_n'

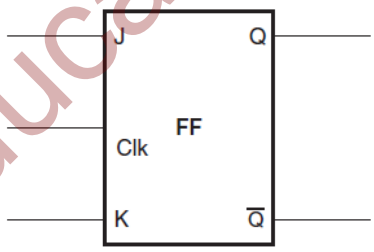
Characteristic table:

Q	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Characteristic Equation:

$$Q_{n+1} = JQ' + K'Q$$

Logic Symbol



Race around condition:

Whenever the width of the trigger pulse is greater than the propagation time of the flip-flop, then flip-flop continues to toggle 1-0-1-0 until the pulse turns 0. When the pulse turns 0, unpredictable output may result i.e. we don't know in what state the output is whether 0 or 1. This is called race around condition.

In level-triggered flip-flop circuits, the circuit is always active when the clock signal is high, and consequently unpredictable output may result. In JK flip-flop, during this active clock period, the output will toggle continuously. The output at the end of the active period is therefore unpredictable. To overcome this problem, *edge-triggered* circuits can be used whose output is determined by the edge, instead of the level, of the clock signal, for example, the rising (or trailing) edge. Master-slave flip-flop is another solution for this problem.

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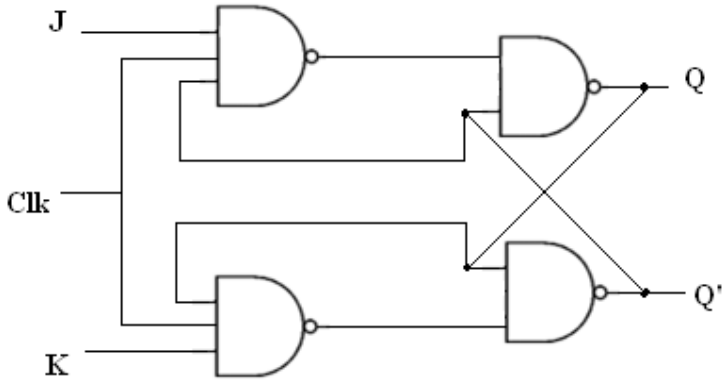
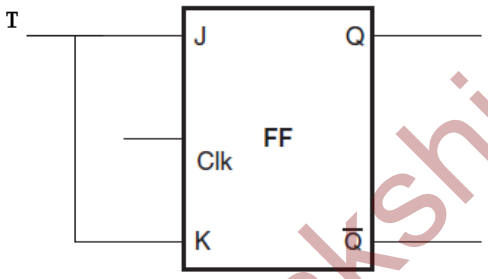
JK Flip-flop using NAND gates:



T flip-flop:

The T flip-flop or Toggle flip-flop is a single input version of the JK flip-flop. The T flip-flop can be obtained from the JK flip-flop when both inputs are tied together.



T	Q_{n+1}
0	Q_n
1	Q_n'

Characteristic table:

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Equation:

$$Q_{n+1} = T'Q_n + TQ_n'$$

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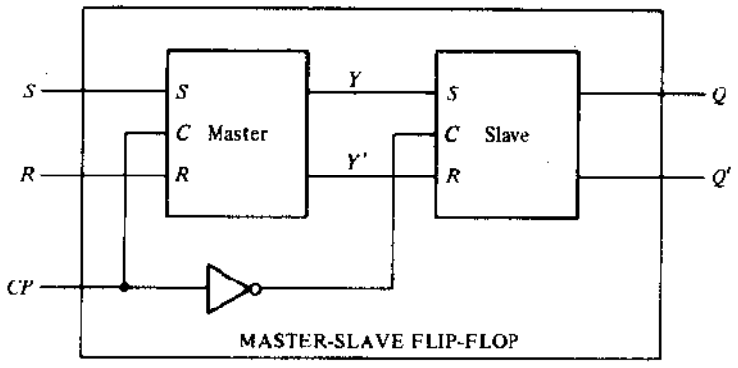
Edge triggering and Level triggering:

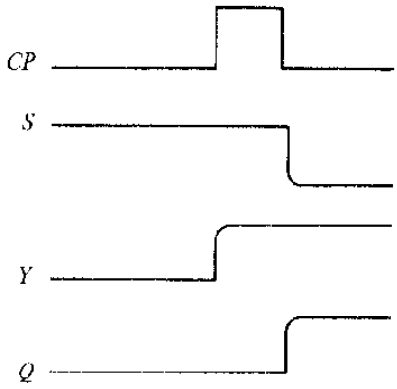
In a *level-triggered* flip-flop, the output responds to the data present at the inputs during the time the clock pulse level is HIGH (or LOW). That is, any changes at the input during the time the clock is active (HIGH or LOW) are reflected at the output as per its function table. In an *edge-triggered* flip-flop, the output responds to the data at the inputs only on LOW-to-HIGH or HIGH-to-LOW transition of the clock signal. The flip-flop in the two cases is referred to as positive edge triggered and negative edge triggered respectively. Any changes in the input during the time the clock pulse is HIGH (or LOW) do not have any effect on the output. The edge triggering can be achieved by using a high pass RC circuit in between the clock and flip-flop. The high pass RC circuit converts the pulses into spikes and the flip-flop can be triggered using these spikes. Another method to achieve edge triggering is master-slave flip-flop.

Master-Slave Flip-flop:

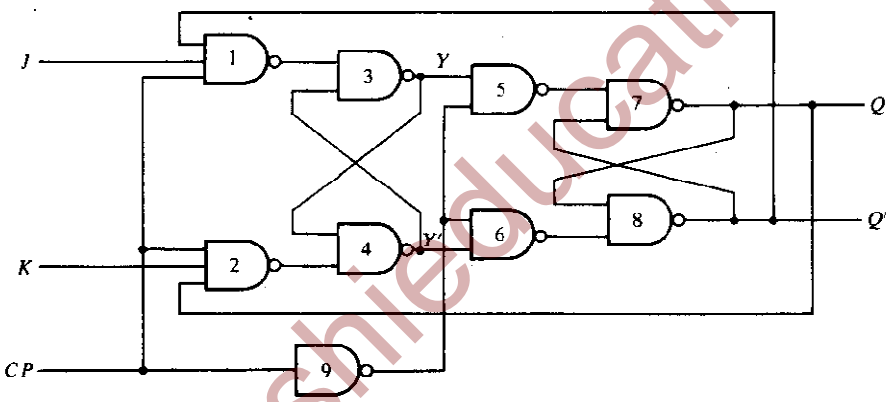
A master-slave flip-flop is constructed from two separate flip-flops in which one circuit acts as a master and the other as a slave. When clock pulse CP is 0, the output of the inverter is 1. Since the clock input of the slave is 1, the flip-flop is enabled and output Q is equal to Y, while Q' is equal to Y'. The master flip-flop is disabled as $CP = 0$. When the pulse becomes 1, the information then at the external S and R inputs is transmitted to the master. When the clock returns to 0 again, the slave accepts the data provided by the master and the external outputs change accordingly.



Timing relationship in Master-slave flip-flop:



***MSJK* Flip-flop with NAND gates:**



It consists of two SR latches, the master and the slave, connected in cascade, as shown in figure. The master is clocked in the normal way, while the clock signal to the slave is inverted. Assuming that changes in the J and K signals are only allowed to occur when the clock is low, the master then being disabled, changes in its output will take place on the rising edge of the clock pulse and these changes are transmitted to the input of the slave. However, no change can occur at the output of the slave until the rising edge of the inverted clock pulse, which is the trailing edge of the clock pulse. Consequently changes in Q and Q' which are fed back to the input of the master do not take place until the trailing edge of the clock pulse arrives. When $J = K = 1$, the transition of Q from 0 to 1 is made on the trailing edge of the clock pulse. The flip-flop will remain in that state until the trailing edge of the next clock pulse when the reverse transition will take place. The flip-flop is

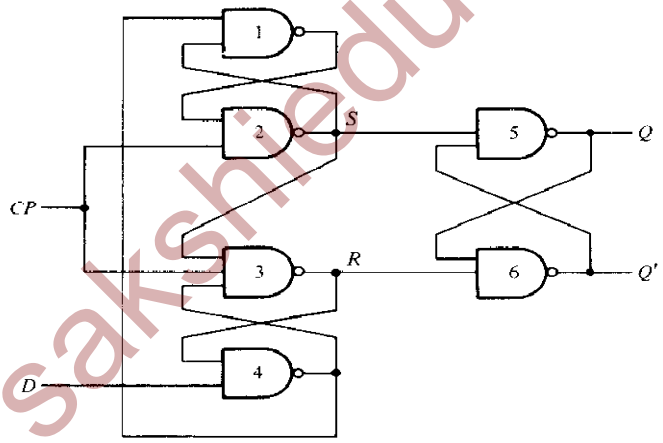
then said to be operating in a toggling mode which is analogous to the unstable oscillatory condition. However, the toggling of Q is now controlled while the condition $J = K = 1$ is maintained, and the flip-flop will toggle on the trailing edge of each successive clock pulse.

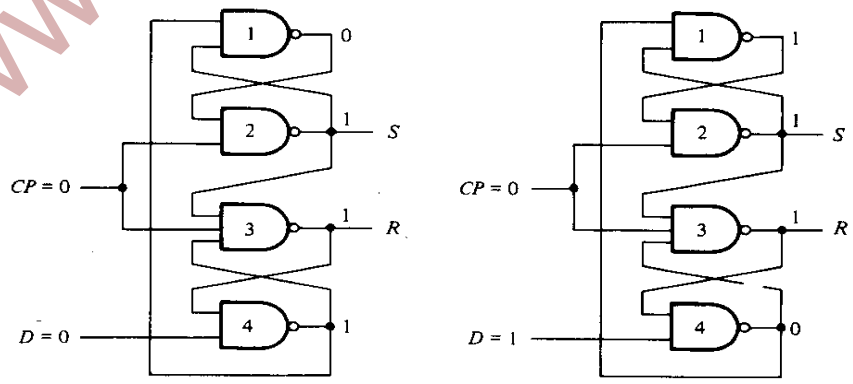
Edge Triggered Flip-flop:

In this type of flip-flop, output transitions occur at a specific level of the clock pulse. Some edge-triggered flip-flops cause a transition on the positive edge of the pulse, and others cause a transition on the negative edge of the pulse.

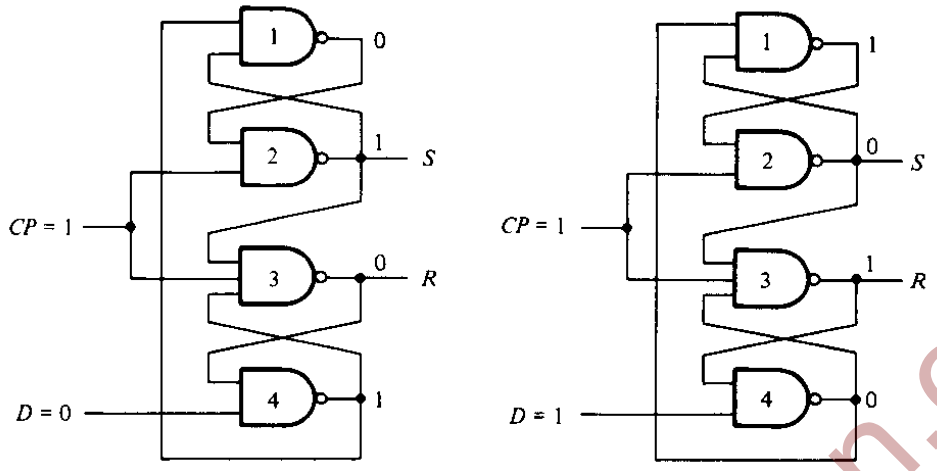
D-type positive edge triggered flip-flop:

It consists of three basic flip-flops or latches, in which 1 and 2 NAND gates form one basic flip-flop and gates 3 and 4 another. The third basic flip-flop comprising gates 5 and 6 provide the outputs to the circuit.





(a) With $CP = 0$



(b) With $CP = 1$

Excitation Tables:

The characteristic table is useful during the analysis of sequential circuits when the value of flip-flop inputs are known and we want to find the value of the flip-flop output Q after the rising edge of the clock signal. As with any other truth table, we can use the map method to derive the characteristic equation for each flip-flop. During the design process we usually know the transition from present state to the next state and wish to find the flip-flop input conditions that will cause the required transition. For this reason we will need a table that lists the required inputs for a given change of state. Such a list is called the excitation table.

SR Flip-flop:

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

JK Flip-flop:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

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D Flip-flop:

	+	
0	0	0
0	1	1
1	0	0
1	1	1

T Flip-flop:

	+	
0	0	0
0	1	1
1	0	1
1	1	0

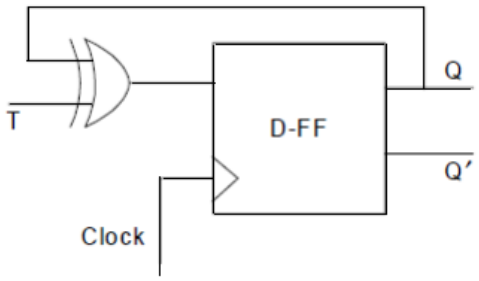
Conversion of Flip-flops:

This section shows how to convert a given type A FF to a desired type B FF using some conversion logic. The key here is to use the excitation table, which shows the necessary triggering signal (S, R, J, K, D and T) for a desired flip flop state transition Q_n to Q_{n+1}.

1. Convert a D flip-flop to a T flip-flop.

T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

$$D = T'Q_n + TQ_n' = T \oplus Q_n$$



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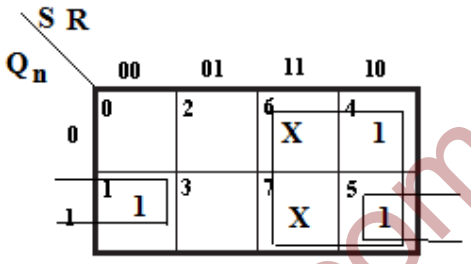
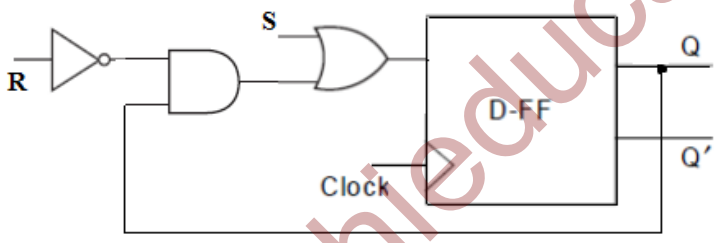
2. Convert SR to D flip-flop.

S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	?	X
1	1	1	?	X



$$D = R'Q_n + S$$



Direct or Asynchronous Inputs:

In many applications, it is desired to initially set or reset the flip-flop, i.e., the initial state of the flip-flop is to be assigned. This is accomplished by using the direct inputs or asynchronous inputs referred to as Preset (Pr) and Clear (Cr or Clr) inputs.

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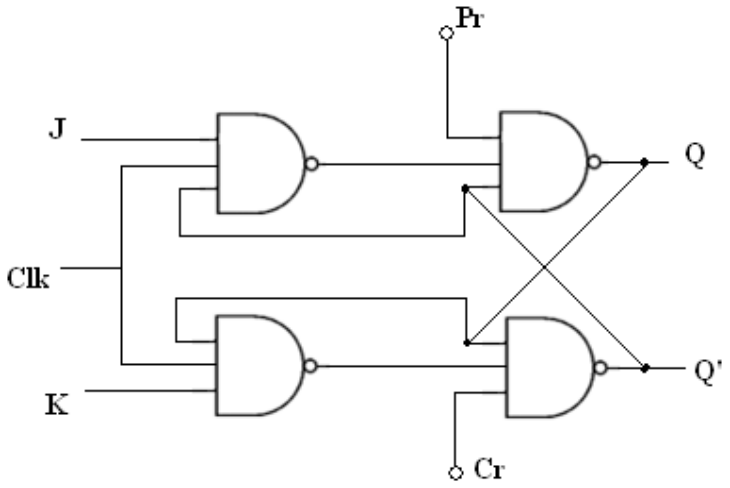

Clk	Pr	Cr	J	K	Q_{n+1}
X	0	1	X	X	1
X	1	0	X	X	0
0	1	1	X	X	Q_n
1	1	1	0	0	Q_n
1	1	1	0	1	0
1	1	1	1	0	1
1	1	1	1	1	Q_n'

With $Pr = 1$ and $Cr = 1$, the flip-flop works normally and the outputs will depend on the inputs. If $Pr = 0$ and $Cr = 1$, the output is in set state irrespective of the inputs. Similarly, if the initial state required is reset state, then apply $Pr = 1$ and $Cr = 0$.

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