Combinational Logic Functions

Decoders & Encoders

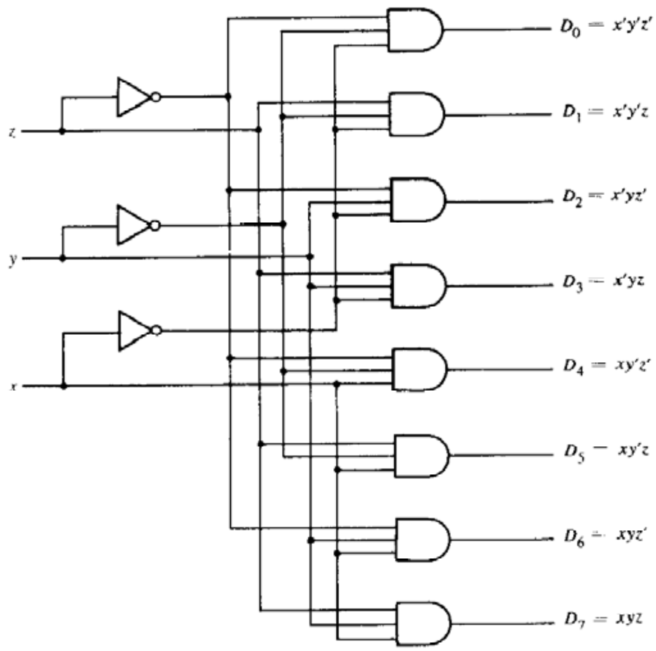
Decoders:

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n-bit decoded information has unused or don't care combinations, the decoder output will have fewer than 2^n outputs. The decoders are called n-to-m line decoders, where $m \leq 2^n$. Their purpose is to generate the 2^n (or fewer) minterms of n input variables.

3×8 Decoder:

In 3×8 decoder or 3-to-8 line decoder, the three inputs are decoded into eight outputs, each output representing one of the minterms of the 3 input variables. It is also known as binary to octal converter. The input variables may represent a binary number, and the outputs will then represent the eight digits in the octal number system.

X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

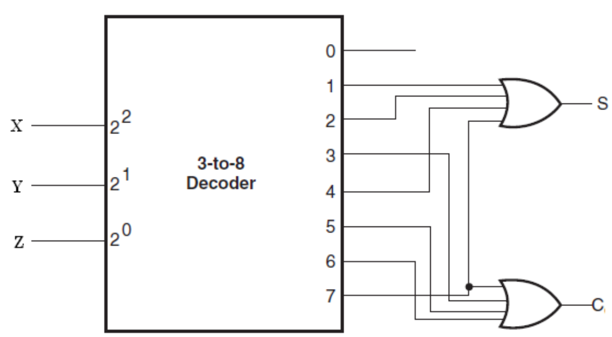


Combinational Logic Implementation:

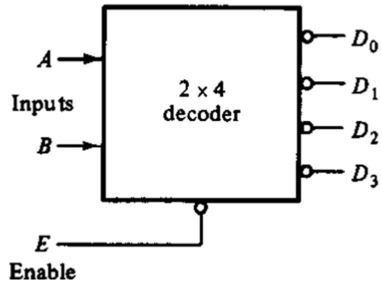
A decoder provides the 2^n minterms of n input variables. Since any Boolean function can be expressed in sum of minterms, one can use a decoder to generate the minterms and an external OR gate to form the sum. In this way, any combinational circuit with n inputs and m outputs can be implemented with an n-to-2^n line decoder and m OR gates.

Example: Implement a Full adder using a decoder and OR gates.

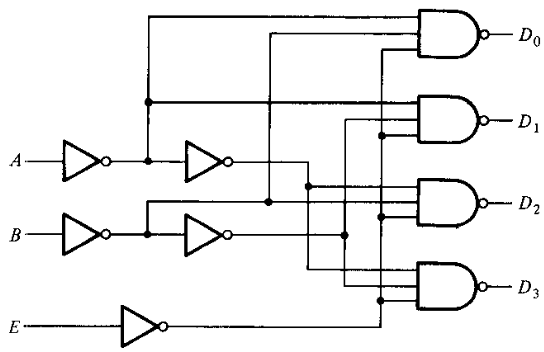
From the truth table of Full adder: $S = \sum m(1,2,4,7)\,, C = \sum m(3,5,6,7)$



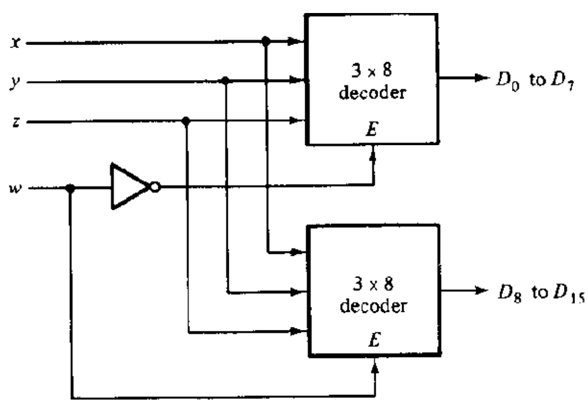
2×4 Decoder with Enable Input:



E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0



4×16 Decoder using 3×8 decoders:



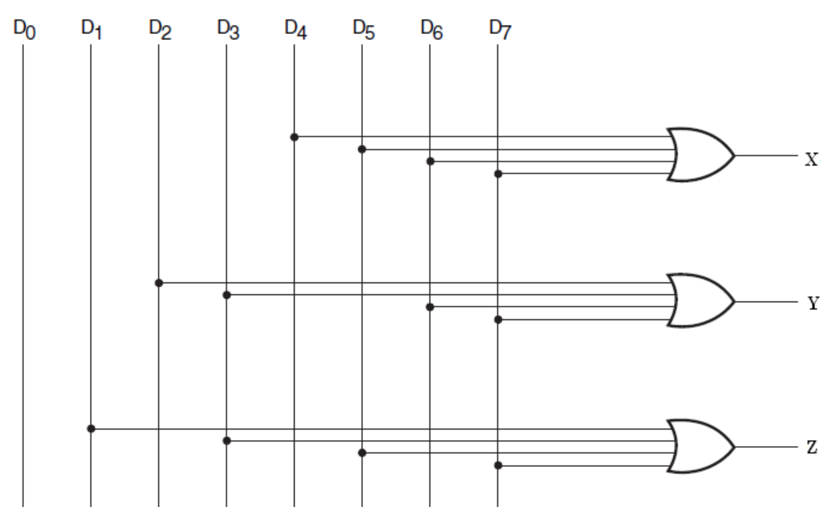
Decoder circuits can be connected to form a larger decoder circuit. When $w = 0$, the top decoder is enabled and the other is disabled. The bottom decoder outputs are all 0's, and the top eight outputs generate minterms 0000 to 0111. When $w = 1$, the bottom decoder is enabled and generate minterms 1000 to 1111, while the outputs of the top decoder are all 0's.

<u>Encoders:</u>

An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n (or fewer) input lines and n output lines. The output lines generate the binary code corresponding to the input value.

Octal to Binary Encoder:

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



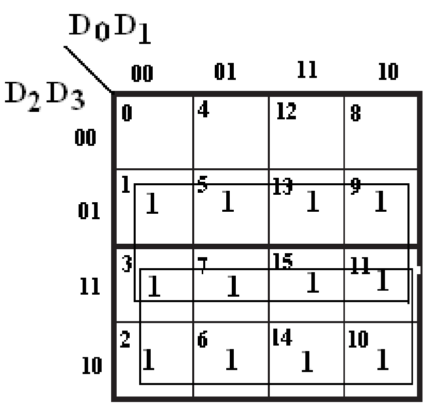
Priority Encoder:

A priority encoder is a practical form of an encoder. The encoders available in IC form are all priority encoders. In this type of encoder, a priority is assigned to each input so that, when more than one input is simultaneously active, the input with the highest priority is encoded.

4-to-2 line Priority Encoder:

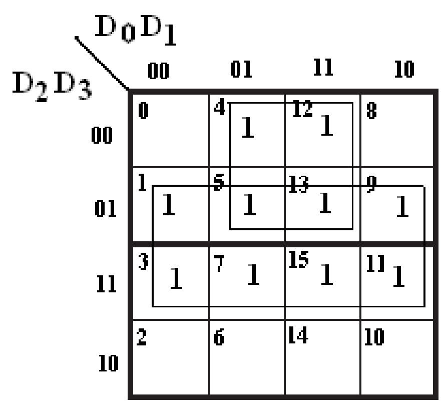
D_0	D_1	D_2	D_3	X	Y
1	0	0	0	0	0
X	1	0	0	0	1
X	X	1	0	1	0
X	X	X	1	1	1

K-map for X:



$$X = D_2 + D_3$$

K-map for Y:



$$Y = D_3 + D_1 D_2'$$