Digital Electronics

Combinational Logic Functions

Carry Look-ahead Adder & Generator

Carry Look-ahead adder:

The addition of two binary numbers in parallel implies that all the bits of the augend and the addend are available for computation at the same time. The total propagation time is equal to the propagation delay of a typical gate times the number of gate levels in the circuit. The longest delay time in a parallel adder is the time it takes the carry to propagate through the full-adders, known as carry propagation time.

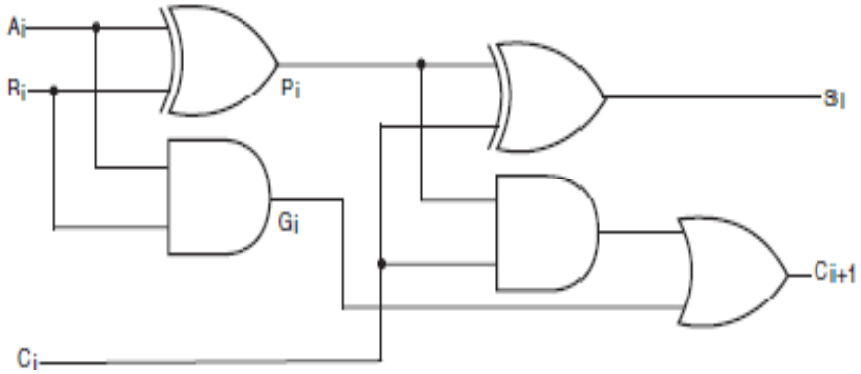
Consider the circuit of the full-adder and we define two new binary variables:

$$P_i = A_i \oplus B_i; G_i = A_i B_i$$

The output sum and carry can be expressed as

$$S_i = P_i \oplus C_i; C_{i+1} = G_i + P_i C_i$$

G_i is called a carry generate and it produces an output carry when both A_i and B_i are one, regardless of the input carry. P_i is called a carry propagate because it is the term associated with the propagation of the carry from C_i to C_{i+1}



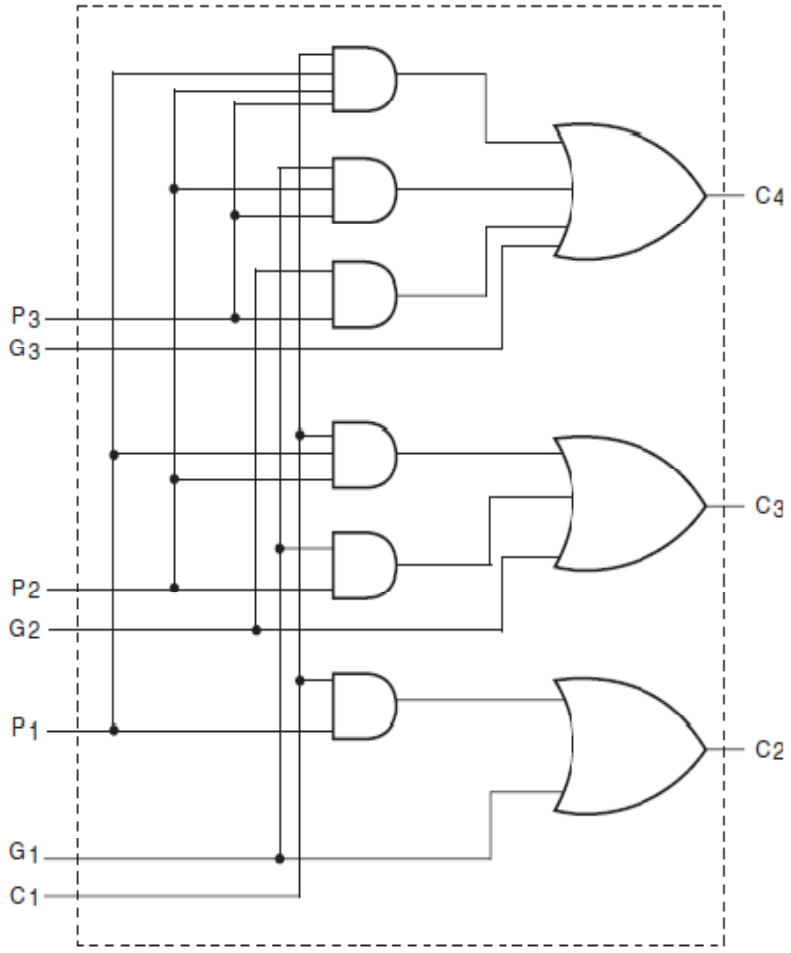
Look-ahead carry generator:

$$C_2 = G_1 + P_1C_1$$

$$C_3 = G_2 + P_2C_2 = G_2 + P_2(G_1 + P_1C_1) = G_2 + P_2G_1 + P_2P_1C_1$$

$$C_4 = G_3 + P_3C_3 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1C_1$$

The three Boolean functions for $C_2, C_3$and C_4 are implemented in the look-ahead carry generator. C_4 does not have to wait for C_3 and C_2 to propagate; and it is propagated at the same time as C_3 and C_2.



The carry look-ahead adder circuit with look-ahead carry generator is as shown.