## Digital Electronics

## Boolean Algebra \& Logic Gates

Logic gates are electronic circuits which can be used to implement the most elementary logical expressions, which are also known as Boolean expressions. The logic gate is the most basic building block of combinational logic.


There are three basic logic gates, namely the OR gate, the AND gate and the NOT gate. Other logic gates that are derived from these basic gates are the NAND gate, the NOR gate, the EXCLUSIVE-OR gate and the EXCLUSIVE-NOR gate.

This chapter deals with logic gates and implementations using NAND and NOR gates followed by simplification of Boolean functions using Boolean Laws and theorems and using K-maps.

## Positive and Negative Logic

The binary variables can have either of the two states, i.e., the logic ' 0 ' state or the logic ' 1 ' state. These logic states in digital systems such as computers, for instance, are represented by two different voltage levels or two different current levels. If the more positive of the two voltage or current levels represents a logic ' 1 ' and the less positive of the two levels represents a logic ' 0 ', then the logic system is referred to as a positive logic system. If the more positive of the two voltage or current levels represents a logic ' 0 ' and the less positive of the two levels represents a logic ' 1 ', then the logic system is referred to as a negative logic system.

If the two voltage levels are 0 V and +5 V , then in the positive logic system the 0 V represents logic ' 0 ' and the +5 V represents logic ' 1 '. In the negative logic system, 0 V represents logic ' 1 ' and 5 V represents logic ' 0 '. If the two voltage levels are 0 V and -5 V , then in the positive logic system the 0 V represents a logic ' 1 ' and the -5 V represents a logic ' 0 '. In the negative logic system, 0 V represents logic ' 0 ' and -5 V represents logic ' 1 '.

## Logic Gates

The Logic Gate is the most basic building block of any digital system, including computers. Each one of the basic logic gates is a piece of hardware or an electronic circuit that can be used to implement some basic logic expression. While laws of Boolean algebra could be used to do manipulation with binary variables and simplify logic expressions, these are actually implemented in a digital system with the help of electronic circuits called logic gates. The three basic logic gates are the OR gate, the AND gate and the NOT gate.

## OR Gate

A logic gate used to perform the operation of logical addition is called an OR gate. An OR gate performs an OR operation on two or more than two logic variables. The OR operation on two independent logic variables $A$ and $B$ is written as $\mathrm{Y}=\mathrm{A}+\mathrm{B}$ and reads as Y equals A OR B. An OR gate is a logic circuit with two or more inputs and one output. The output of an OR gate is LOW only when all of its inputs are LOW. For all other possible input combinations, the output is HIGH. A truth table lists all possible combinations of input binary variables and the corresponding outputs of a logic system. Figure shows the circuit symbol and the truth table of a two-input OR gate. The operation of a two-input OR gate is explained by the logic expression

$$
\mathrm{Y}=\mathrm{A}+\mathrm{B}
$$



| A | B | Y |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

## Two input OR Gate

## AND Gate

A logic gate used to perform logical multiplication is known as AND gate. An AND gate is a logic circuit having two or more inputs and one output. The output of an AND gate is HIGH only when all of its inputs are in the HIGH state. In all other cases, the output is LOW. The logic symbol and truth table of a two-input AND gate is shown in figure. The AND operation on two independent logic variables $A$ and $B$ is written as $Y=A . B$ and reads as $Y$ equals $A$ AND $B$. The operation of a two-input AND gate is explained by the logic expression

$$
Y=A . B
$$



Two input AND Gate

## NOT Gate

A logic gate used to perform logical inversion is known as a NOT gate. A NOT gate is a one-input, one-output logic circuit whose output is always the complement of the input. That is, a LOW input produces a HIGH output, and vice versa. If $X$ is the input to a NOT circuit, then its output Y is given by $\mathrm{Y}=\bar{X}$ or $X^{\prime}$ and reads as Y equals NOT $X$. The logic symbol and truth table of a NOT gate is shown in figure. The operation of a NOT gate is explained by the logic expression

$$
\mathrm{Y}=\bar{X}
$$



## NOT Gate

## NAND Gate

NAND stands for NOT AND. An AND gate followed by a NOT circuit makes it a NAND gate. The output of a NAND gate is logic ' 0 ' when all its inputs are logic ' 1 '. For all other input combinations, the output is logic ' 1 '. The symbol and truth table of a NAND gate is as shown. NAND gate operation is logically expressed as

$$
Y=\overline{A B}
$$



## Two input NAND Gate

NAND Gate is known as Universal gate as it can be used alone to implement any gate operation. Hence it is said to be functionally complete.

## NOR Gate

NOR stands for NOT OR. An OR gate followed by a NOT circuit makes it a NOR gate. The output of a NOR gate is logic ' 1 ' when all its inputs are logic ' 0 '. For all other input combinations, the output is logic ' 0 '. The symbol and truth table of a NOR gate is as shown. The output of a two-input NOR gate is logically expressed as

$$
Y=(\overline{A+B)}
$$



| A | B | Y |
| :---: | :---: | :---: |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Two input NOR Gate

NOR gate is also known as Universal gate as it is used alone to implement any gate operation and hence it is also functionally complete.

## EXCLUSIVE-OR Gate

The EXCLUSIVE-OR gate, commonly written as EX-OR gate, is a two-input, one-output gate. The output of an EX-OR gate is logic ' 1 ' when the inputs are unlike and logic ' 0 ' when the inputs are like. Although EX-OR gates are available in integrated circuit form only as two-input gates, unlike other gates which are available in multiple inputs also, multiple-input EX-OR logic functions can be implemented using more than one two-input gates. The output of a multiple-input EX-OR logic function is logic ' 1 ' when the number of 1 s in the input sequence is odd and logic ' 0 ' when the number of 1 s in the input sequence is even, including zero. The symbol and truth table of an EX-OR gate is shown in figure. The output of a two-input EX-OR gate is logically expressed as

$$
Y=A \oplus B=A^{\prime} B+A B^{\prime}
$$



## Two input EX-OR Gate

## EXCLUSIVE-NOR Gate

EXCLUSIVE-NOR, commonly written as EX-NOR, means NOT of EX-OR, i.e., the logic gate that we get by complementing the output of an EX-OR gate. The truth table of an EX-NOR gate is obtained from the truth table of an EX-OR gate by complementing the output entries as shown in figure. Logically,

$$
Y=\overline{A \oplus B}=A^{\prime} B^{\prime}+A B
$$



| A | B | Y |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## Two input EX-NOR Gate

The output of a two-input EX-NOR gate is logic ' 1 ' when the inputs are like and logic ' 0 ' when they are unlike. In general, the output of a multiple-input EX-NOR logic function is logic ' 0 ' when the number of 1 s in the input sequence is odd and a logic ' 1 ' when the number of 1 s in the input sequence is even including zero.

## Boolean algebra:

Boolean algebra is an algebraic structure defined on a set of elements B together with two binary operators + and $\cdot$ provided the following postulates are satisfied:

1. a) Closure with respect to the operator + .
b) Closure with respect to the operator $\cdot$.
2. a) An identity element with respect to + , designated by $0: x+0=0+x=x$.
b) An identity element with respect to ', designated by 1: $x \cdot 1=1 \cdot x=x$.
3. a) Commutative with respect to $+: x+y=y+x$.
b) Commutative with respect to $\cdot x \cdot y=y \cdot x$.
4. a) is distributive over $+: x \cdot(y+z)=(x \cdot y)+(x \cdot z)$.
b) + is distributive over $: x+(y \cdot z)=(x+y) \cdot(x+z)$.
5. For every element $x \in B$, there exists an element $x^{\prime} \in B$ (complement of $x$ ) such that

$$
x+x^{\prime}=1 \text { and } x \cdot x^{\prime}=0
$$

## Boolean Laws \& Theorems:

## Duality Principle:

It states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged. If the
dual of an algebraic expression is desired, OR and AND operators are interchanged and 1's are replaced by 0's and 0's by 1 's.

1. a) $x+0=x \quad$ b) $x \cdot 1=x$
2. a) $x+x^{\prime}=1$
b) $x \cdot x^{\prime}=0$
3. a) $x+x=x$
b) $x \cdot x=x$
4. a) $x+1=1$
b) $x \cdot 0=0$
5. DeMorgan's Theorem: $a)(x+y)^{\prime}=x^{\prime} y^{\prime} \quad$ b) $(x y)^{\prime}=x^{\prime}+y^{\prime}$
6. Absorption Theorem:
a) $x+x y=x$
b) $x(x+y)=x$

## Simplification using Boolean Laws \& Theorems:

The Boolean functions can be simplified by using appropriate Boolean laws and theorems.

## Examples:

Simplify the following functions using Boolean laws and theorems:

1. $F=A B C D+A B C^{\prime} D^{\prime}+A B C D^{\prime}+A B C^{\prime} D+A B C D E+A B C^{\prime} D^{\prime} E^{\prime}+$ $A B C^{\prime} D E$

Sol: $\quad F=A B C D+A B C^{\prime} D^{\prime}+A B C D^{\prime}+A B C^{\prime} D+A B C D E+A B C^{\prime} D^{\prime} E^{\prime}+$ $A B C^{\prime} D E$

$$
\begin{aligned}
&=A B C\left(D+D^{\prime}\right)+A B C^{\prime}\left(D+D^{\prime}\right)+A B D E\left(C+C^{\prime}\right)+A B C^{\prime} D^{\prime} E^{\prime} \\
&=A B\left(C+C^{\prime}\right)+A B D E+A B C^{\prime} D^{\prime} E^{\prime}=A B\left(1+D E+C^{\prime} D^{\prime} E^{\prime}\right)=A B
\end{aligned}
$$

2. $F=x y+x^{\prime} z+y z$

Sol:

$$
\begin{aligned}
& F=x y+x^{\prime} z+y z \\
& =x y+x^{\prime} z+y z\left(x+x^{\prime}\right)=x y(1+z)+x^{\prime} z(1+y) \\
& =x y+x^{\prime} z
\end{aligned}
$$

3. $F=A B C+A^{\prime} B^{\prime} C+A^{\prime} B C+A B C^{\prime}+A^{\prime} B^{\prime} C^{\prime}$

Sol: $F=A B C+A^{\prime} B^{\prime} C+A^{\prime} B C+A B C^{\prime}+A^{\prime} B^{\prime} C^{\prime}$

$$
=B C+A^{\prime} B^{\prime}+A B C^{\prime}=B\left(C+A C^{\prime}\right)+A^{\prime} B^{\prime}=A B+B C+A^{\prime} B^{\prime}
$$

## Universal Gates

OR, AND and NOT gates are the three basic logic gates as they together can be used to construct the logic circuit for any given Boolean expression. NOR and NAND gates have the property that they individually can be used to hardwareimplement a logic circuit corresponding to any given Boolean expression. That is, it is possible to use either only NAND gates or only NOR gates to implement any Boolean expression. This is so because a combination of NAND gates or a combination of NOR gates can be used to perform functions of any of the basic logic gates. It is for this reason that NAND and NOR gates are universal gates.

## Implementation of gates using NAND gates

a) NOT gate:

b) AND gate:

c) OR gate:


## d) NOR gate:


e) Ex-OR gate:

f) Ex-NOR gate:


Implementation of gates using NOR gates
a) NOT gate:

b) AND gate:

c) OR gate:

d) NAND gate:

e) Ex-OR gate:

f) Ex-NOR gate:


## IEEE/ANSI Symbols:







## Boolean Expressions:

A Boolean expression or a function is an expression which consists of binary variables joined by the Boolean connectives AND and OR along with NOT operation.

Any Boolean expression can be expressed in two forms:
a) Canonical form
b) Standard form

## Canonical Form:

An expanded form of Boolean expression, where each term contains all Boolean variables in their true or complemented form, is known as the canonical form of the expression.
a) Sum of minterms: Any Boolean function can be expressed as a sum of minterms expression. A minterm is a standard product which consists of all variables in either complemented or un-complemented form for which the output is 1 . For example,

$$
\begin{aligned}
& Y=A^{\prime} B C+A B^{\prime} C^{\prime}+A B C \\
& =\sum m(3,4,7)
\end{aligned}
$$

is a sum of minterms expression with three variables.
b) Product of maxterms: Any Boolean function can be expressed as a product of maxterms expression. A maxterm is a standard sum which
consists of all variables in either complemented or un-complemented form for which the output is 0 . For example,

$$
\begin{aligned}
& \quad Y=\left(A^{\prime}+B^{\prime}+C\right)\left(A+B+C^{\prime}\right)(A+B+C) \\
& =\prod M(0,1,6)
\end{aligned}
$$

is a product of maxterms expression with three variables.

## Standard Form:

A simplified form of a Boolean expression which may consist of one or more number of variables in each term in either complemented or un-complemented form is known as Standard form of the expression.
a) Sum of Products (SOP): The sum of products is a Boolean expression containing AND terms, called Product terms, of one or more literals each; the sum denotes the ORing of these terms. For example,

$$
Y=A^{\prime} B+B C^{\prime}+A C
$$

is a SOP expression with three variables.
b) Product of Sums (POS): It is a Boolean expression containing OR terms called Sum terms and the product denotes the ANDing of these terms.

$$
Y=A\left(A+B^{\prime}\right)\left(B+C^{\prime}\right)
$$

is a POS expression with three variables.
** Canonical form is obtained when a function is taken from a truth table. When implementing a Boolean function with gates, standard form is preferred.

## Simplification of Boolean expressions:

The primary objective of all simplification procedures is to obtain an expression that has the minimum number of terms. Obtaining an expression with the minimum number of literals is usually the secondary objective. The Boolean functions can be simplified by using
a) Boolean Laws and theorems
b) K maps
c) Quine Mc-Cluskey or Tabulation Method

## Simplification using K-maps:

A Karnaugh map is a graphical representation of the logic system. It can be drawn directly from either minterm (sum-of-products) or maxterm (product-of-sums) Boolean expressions. Drawing a Karnaugh map from the truth table involves an additional step of writing the minterm or maxterm expression depending upon whether it is desired to have a minimized sum-of-products or a minimized product of sums expression.

An n-variable Karnaugh map has $2^{\mathrm{n}}$ squares, and each possible input is allotted a square. In the case of a minterm Karnaugh map, ' 1 ' is placed in all those squares for which the output is ' 1 ', and ' 0 ' is placed in all those squares for which the output is ' 0 '. Os are omitted for simplicity. An ' X ' is placed in squares corresponding to 'don't care' conditions.
a) Two Variable K-map:

i) Sum of minterms representation
ii) Product of maxterms representation
b) Three Variable K-map:

i) Sum of minterms representation

ii) Product of maxterms representation
c) Four Variable K-map:

i) Sum of minterms representation

ii) Product of maxterms representation
d) Five Variable K-map:


## Simplification Algorithm:

Simplification of logical functions using K-maps is based on the principle of combining terms in adjacent cells. Two cells are said to be adjacent if they differ in only one variable.

1. Identify the ones which cannot be combined with any other ones and encircle them. These are called essential prime implicants.
2. Identify the ones that can be combined in groups of two in only one way. Encircle them.
3. Identify the ones that can be combined with three other ones, to make a group of four adjacent ones, in only one way. Encircle such group of ones.
4. Identify the ones that can be combined with seven other ones, to make a group of eight adjacent ones, in only one way. Encircle them.
5. After identifying the essential groups of 2,4 , and 8 ones, if there still remain some ones which have not been encircled, then these are to be combined with each other or with other already encircled ones.

Examples:

1. Simplify the Boolean function $F=A^{\prime} C+A^{\prime} B+A B^{\prime} C+B C$

Sol: $F=A^{\prime} C+A^{\prime} B+A B^{\prime} C+B C=A^{\prime} B^{\prime} C+A^{\prime} B C^{\prime}+A^{\prime} B C+A B^{\prime} C+A B^{\prime} C$

|  | $\begin{gathered} \overline{\mathrm{A}} \overline{\mathrm{~B}} \\ \mathbf{0 0} \\ \hline \end{gathered}$ | $\begin{gathered} \text { A B } \\ 01 \end{gathered}$ | $\begin{gathered} \text { A B } \\ 11 \end{gathered}$ | $\begin{gathered} A \bar{B} \\ 10 \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: |
| C 0 | 0 | $\sqrt[2]{1}$ | 6 | 4 |
| C 1 | 1 | 31 | 7 | 5 |

$$
F=C+A^{\prime} B
$$

2. $F(A, B, C, D)=\sum m(0,1,2,3,5,7,8,9,11,14)$

|  | $\overline{\mathrm{A}} \overline{\mathrm{B}}$ <br> 00 | $\begin{aligned} & \bar{A} B \\ & 01 \end{aligned}$ | $\begin{gathered} \mathrm{AB} \\ 11 \end{gathered}$ | $\begin{gathered} A \bar{B} \\ 10 \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: |
| CD 00 | 0 | ${ }^{4}$ | 12 | $\sqrt{8}_{1}$ |
| CD 01 | ${ }^{1} 1$ | 1 | 13 | ${ }^{9} 1$ |
| CD ${ }^{1}$ | ${ }^{3} 1$ | ${ }^{7} 1$ | 15 | ${ }^{11} 1$ |
| CD 10 | 2 | ${ }^{6}$ | ${ }^{14}$ (1) | 10 |

$$
F=A^{\prime} B^{\prime}+A^{\prime} D+A B C D^{\prime}+B^{\prime} C^{\prime}+B^{\prime} D
$$

3. $F(A, B, C, D)=\sum m(1,2,3,5,7,8,9,10,13)$

|  | $\begin{aligned} & \bar{A} \bar{B} \\ & 00 \end{aligned}$ | $\begin{gathered} \bar{A} B \\ 01 \end{gathered}$ | $\mathrm{AB}$ | $A \bar{B}$ |
| :---: | :---: | :---: | :---: | :---: |
| CD 00 | 0 | 4 | 12 | ${ }^{8} 1$ |
| CD 01 | $\sqrt{1}$ | 5 | 13 | 1 |
| CD 11 | 3 | 1 | 15 | 11 |
| CD 10 | 2 | 6 | 14 | $\sqrt{10}_{1}$ |

$$
F=A^{\prime} C D+A C^{\prime} D+A B^{\prime} D^{\prime}+A^{\prime} B^{\prime} D+A^{\prime} B^{\prime} C
$$

4. $F(A, B, C, D)=\Pi M(0,1,2,3,4,10,11)$


$$
F=(A+B)(A+C+D)\left(B+C^{\prime}\right)
$$

5. $F=\sum m(1,2,3,5,13)+\sum d(6,7,8,9,11,15)$


$$
F=D+A^{\prime} C
$$

6. $F=\sum m(0,2,4,9,12,15)+\sum \emptyset(1,5,7,10)$


## Two level Implementation:

Any logic circuit can be implemented in two levels by representing the Boolean function either in SOP or POS form. Two level NAND and NOR circuits can be obtained by representing the expression in SOP and POS form respectively. Minimum propagation delay will be obtained by using two level implementation. But as the number of terms increases, the number of inputs increases for the second level gate.

## NAND Implementation:

By expressing the given function in SOP form, the logic circuit can be implemented using two level NAND gates.

Example:
Implement $Y=A\left(A^{\prime}+B^{\prime}\right)+B C^{\prime}+A C$ using NAND gates.
Sol:

$$
\begin{aligned}
Y & =A\left(A^{\prime}+B^{\prime}\right)+B C^{\prime}+A C \\
& =A B^{\prime}+B C^{\prime}+A C \quad \text {----- SOP form }
\end{aligned}
$$

By using double complements we get,

$$
Y=\left(Y^{\prime}\right)^{\prime}=\left\{\left(A B^{\prime}+B C^{\prime}+A C\right)^{\prime}\right\}^{\prime}=\left(A B^{\prime}\right)^{\prime}\left(B C^{\prime}\right)^{\prime}(A C)^{\prime}
$$



## NOR Implementation:

By expressing the given function in POS form, the logic circuit can be implemented using two level NOR gates.

Example:
Implement $Y=A^{\prime} B+B C^{\prime}$ using NOR gates.
Sol:

$$
\begin{aligned}
Y= & A^{\prime} B+B C^{\prime} \\
& =\left(A^{\prime} B+B\right)\left(A^{\prime} B+C^{\prime}\right) \ldots \ldots . \text { Distributive law } \\
Y= & B\left(A^{\prime}+B\right)\left(A^{\prime}+C^{\prime}\right)\left(B+C^{\prime}\right) \ldots \ldots . \text { Distributive law }
\end{aligned}
$$

and the expression is in POS form.

$$
\begin{aligned}
& Y=\left(Y^{\prime}\right)^{\prime}=\left[\left\{B\left(A^{\prime}+B\right)\left(A^{\prime}+C^{\prime}\right)\left(B+C^{\prime}\right)\right\}^{\prime}\right]^{\prime} \\
& =\left[(B)^{\prime}+\left(A^{\prime}+B\right)^{\prime}+\left(A^{\prime}+C^{\prime}\right)^{\prime}+\left(B+C^{\prime}\right)\right]^{\prime}
\end{aligned}
$$

## Multilevel Implementation:

Multi level NAND or NOR implementation of a Boolean circuit can be achieved by replacing each gate in the circuit with the NAND or NOR equivalent circuits respectively. With this type of implementation, very large propagation delay is achieved and only two input gates are required.

## NAND Implementation:

By replacing each gate in the circuit with the NAND equivalent, multi level NAND circuit is achieved. When two single input NAND gates (inverters) are in series, they can be removed.

Example: $Y=A(B+C D)+B C^{\prime}$



NOR Implementation:
By replacing each gate in the circuit with the NOR equivalent, multi level NOR circuit is achieved. When two single input NOR gates (inverters) are in series, they can be removed.

Example: $Y=A(B+C D)+B C^{\prime}$


