Digital Electronics

Multiple Choice Questions

Answers option is in **Bold** letters

Chapter 1 : Number Systems & Codes

1. What is the binary equivalent of the decimal number 368

   (A) 101110000 (B) 110110000 (C) 111010000 (D) 111100000

2. The decimal equivalent of hex number 1A53 is

   (A) 6793 **(B)** 6739 (C) 6973 (D) 6379

3. $(734)_8 = (\quad)_{16}$

   (A) C 1 D (B) D C 1 (C) 1 C D **(D)** 1 D C

4. The hexadecimal number 'A0' has the decimal value equivalent to

   (A) 80 (B) 256 (C) 100 **(D)** 160

5. The 2's complement of the number 1101101 is

   (A) 0101110 (B) 0111110 (C) 0110010 **(D)** 0010011

6. -8 is equal to signed binary number

   (A) 10001000 (B) 00001000 (C) 10000000 (D) 11000000

7. The decimal equivalent of Binary number 11010 is

   (A) 26 (B) 36 (C) 16 (D) 23

8. The number 140 in octal is equivalent to

   (A) $(96)_{10}$ (B) $(86)_{10}$ (C) $(90)_{10}$ (D) none of these

9. The result of adding hexadecimal number A6 to 3A is

   (A) DD **(B)** E0 (C) F0 (D) EF

10. Converting $(153)_{10}$ to base 8 yields which of the following results?

    (A) 107 (B) 132 (C) 701 (D) 231

11. Converting $(153)_8$ to base 10 yields which of the following results?

    (A) 107 (B) 132 (C) 701 (D) 231

12. In 1's complement addition the carry generated at the last stage taken as end around carry is

(A) Neglected (B) connected to the input of first stage

(C) Stored in the sign bit (D) None of the above

13. In 2's complement addition the carry generated at the last stage taken as end around carry is

(A) Neglected (B) connected to the input of first stage

(C) Stored in the sign bit (D) none of the above

14. The number 64_{10} is equivalent to the binary number:

(A) 1000000 (B) 1010000101 (C) 1011101001 (D) None

15. The two's complement of an odd number always

(A)ends with a one (B) ends with a zero

(C) starts with a zero (D) starts with a one.

16. The result of 1101110101_2-1111_2 is:

(A) 870_{10} (B) 678_{10} (C) 101110101_2 (D) 1101110111_2

17. Thetwo'sComplement of 101011001110 is

(A) 010100110110 (B) 101011001111 (C) 100100110001 **(D)** 010100110010

18. Conversion from decimal to hexadecimal requires repeated division by

(A) 16 (B) 4 (C) 10 (D) 8

19. The Gray code for decimal number 6 is equivalent to

(A) 1100 (B) 1001 **(C)** 0101 (D) 0110

20. The code where all successive numbers differ from their preceding number by single bit is

(A) Binary code (B) BCD (C) Excess – 3 **(D)** Gray

21. The excess 3 code of decimal number 26 is

(A) 0100 1001 **(B)** 01011001 (C) 1000 1001 (D) 01001101

22. A Hamming code 1010101 was received. What is the received data?

(A)1000 (B)1101 (C) 1010 (D) 0101

23. In 8421 BCD code, the decimal number125 is written as

(A) 1111101 (B) 000100100101 (C) 7D (D) None

24. Binary Coded Decimal (BCD) numbers express each decimal digit as a

(A) bit (B) byte (C) nibble (D) None

25. ASCII code is an alphanumeric code with

(A) 4 bits (B) 7 bits (C) 6 bits (D) 2 bits

26. EBCDIC code is an alphanumeric code with

(A) 4 bits (B) 7 bits **(C)** 8 bits (D) 2 bits

27. The self-complementing code among the following is

(A) 2421 (B) 8421 (C) 3322 (D) Gray code

28. Which of the following is a non-weighted code?

(A) 2421 **(B)** Excess-3 (C) 8421 (D) 5211

29. Pick out the code from the following which is not a self-complementing code

(A) 3321 **(B)** 8421 (C) 2421 (D) 642-3

30. The sequential code among the following is

(A) BCD (B) Excess 3 **(C)** both (D) Gray code

Chapter 2: Boolean algebra & Logic families

1. The NAND gate output will be low if the two inputs are

   (A) 00 (B) 01 (C) 10 **(D)** 11

2. The output of a logic gate is 1 when all its inputs are at logic 0. The gate is either

   (A) a NAND or an EX-OR (B) an OR or an EX-NOR

   (C) an AND or an EX-OR **(D)** a NOR or an EX-NOR

3. DeMorgan's first theorem shows the equivalence of

   (A) OR gate and Exclusive OR gate **(B)** NOR gate and Bubbled AND gate

   (C) NOR gate and NAND gate (D) NAND gate and NOT gate

4. In a positive logic system, logic state 1 corresponds to

   (A) positive voltage **(B)** higher voltage level

   (C) zero voltage level (D) lower voltage level

5. The OR gate output will be low if the two inputs are

   (A) 00 (B) 01 (C) 10 (D) 11

6. When an input signal A=11001 is applied to a NOT gate serially, its output signal is

   (A) 00111 **(B)** 00110 (C) 10101 (D) 11001

7. A universal logic gate is one, which can be used to generate any logic function. Which of the following is a universal logic gate?

   (A) OR (B) AND (C) XOR **(D)** NAND

8. An EX-OR gate gives a high output

   (A) if there are odd number of 1s (B) if it has even number of 1s

   (C) if the decimal value of digital word is even (D) for odd decimal value

9. Bubbled OR gate is equal to----------.

   a) AND (B) NOR **(C)** NAND (D) None

10. An equivalent representation for the Boolean expression A' + 1 is

    (A) A (B) A' **(C)**1 (D) 0

11. An equivalent representation for the Boolean expression A + A' is

(A) A (B) A' **(C)**1 (D) 0

12. Simplification of the Boolean expression AB + A(BC)' yields which of following results?

(A) A (B) BC (C) B (D) AB

13. Simplifying (AB)' + A'B to most basic form yields which of the following expressions?

(A) A' (B) B' (C) B **(D)** (AB)'

14. The expression A' + B' + C is represented by which of the following canonical symbols?

(A) M_1 (B) M_6 (C) m_1 (D) m_6

15. A 2-input gate has inputs of A= 1 and B = 0; if the output is a 1, the gate could be:

(A) an AND, ENOR or a NOR gate. (B) an AND, XOR or an NOR gate.

(C) a NAND, XOR or an OR gate. (D) a NAND, XNOR or an OR gate

16. Which one of the following is the odd one out?

(A) C + AB (B) A.B + C (C) (A.(B) + C **(D)** A.(C + (B)

17. The least number of gates that could be used to build alogic circuit with the Boolean expression (A + B + (C)' would be:

(A) 1 (B) 2 (C) 3 (D) 4

18. Which of the following statements represent Commutative law?

(A) A+(B+(C) = (A+(B)+C **(B)** A+B=B+A

(C) A(B+(C)=AB+AC (D) None

19. Which of the following gates is known as Equality detector?

(A) OR gate (B) AND (C) NOT **(D)** Ex-NOR

20. Which of the following operations is not associative?

(A) EX-OR (B) AND **(C)** NOR (D) OR

21. A literal is a

(A) primed variable **(B)** primed or un primed variable

(C) un primed variable (D) None

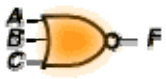
22. Which one of the following is De-Morgan's theorem?

(A) (A+B)' = A'+B' **(B)** (A+B)' = A'.B' (C) Both (D) (A.B)' = A'.B'

23. Minterm m_{31} must be represented by at least how many literals?

(A) 6 (B) 31 (C) 3 **(D)** 5

24. Which of the following canonical expressions is generated by the NOR gate shown?



(A) $F = m_0$ (B) $F = M_0$ (C) $F = m_7$ (D) $F = M_7$

25. The number of rows in a truth table of n variables is

(A) 2n (B) n (C) n^3 **(D)** n^2

26. The reduced SOP for the expression $F(A, B, C)=\sum m(0, 1, 5) + \sum d(4,7)$ is

(A) B' (B) 0 (C) A' (D) 1

27. An Ex-OR gate can be used as a NOT gate if

(A) one input is constant at logic 1 (B) one input is constant at logic 0

(C) both of the above (D) None of the above

28. The given max term is A+B+C, its equivalent binary representation is

(A) 111 (B) 101 **(C)** 000 (D) 010

29. The logic gate that will produce a HIGH output whenever the two inputs are at opposite logic levels is the

(A) Exclusive OR (B) Exclusive NOR (C) NOR (D) NAND

30. The basic logic device that always has a single input is the

(A) OR gate (B) Comparator (C) AND gate **(D)** Inverter.

31. NAND gates are preferred over others because these

(A) have lower fabrication area **(B)** can be used to make any gate

(C) consume least electronic power (D) provide maximum density in a chip.

32. An AND gate will function as OR if

(A) all the inputs to the gates are "1" (B) all the inputs are '0'

(C) either of the inputs is "1" **(D)** all the inputs and outputs are complemented

33. Implementation of the Boolean expression $X = ABC + AB + AC'$ results in _____.

(A) three AND gates, one OR gate

(B) three AND gates, one NOT gate, one OR gate

(C) three AND gates, one NOT gate, three OR gates

(D) three AND gates, three OR gates

34. How many 2-input NOR gates does it take to produce a 2-input NAND gate?

(A) 1 (B) 2 (C) 3 **(D)** 4

35. A logic circuit with an output$X = A'BC + AB'$ consists of _____.

(A) two AND gates, two OR gates, two inverters

(B) three AND gates, two OR gates, one inverter

(C) two AND gates, one OR gate, two inverters

(D) two AND gates, one OR gate

36. The output of an exclusive-NOR gate is 1. Which input combination is correct?

(A) A=1, B=0 (B) A=0, B=1 **(C)** A=0, B=0 (D) None

37. How many NOT gates are required to implement the Boolean expression,$X = AB'C + A'BC$?

(A) 1 **(B)** 2 (C) 4 (D) 5

38.Karnaugh map is used for the purpose of

(A) Reducing the electronic circuits used

(B) To map the given Boolean logic function

(C) To minimize the terms in a Boolean expression

(D) To maximize the terms of a given a Boolean expression

39.A reduction in the number of gates can be achieved by using the:

(A) identities or the commutative law. (B) the commutative and the associative laws.

(C) identities or the distributive law. (D) identities but none of the other laws.

40. Which of the following logic families has the shortest propagation delay?

(A) CMOS (B) ECL (C) TTL (D) HTL

41. Why must CMOS devices be handled with care?

(A)so they don't get dirty (B) because they break easily

(C)because they can be damaged by static electricity discharge (D) none

42. What is the major advantage of ECL logic?

(A) very high speed (B) wide range of operating voltage

(C) very low cost (D)very high power

43. What is the range of invalid TTL output voltage?

(A) 0.0–0.4 V **(B)** 0.4–2.4 V (C) 2.4–5.0 V (D) 0.0–5.0 V

44. What should be done with unused inputs to a TTL NAND gate?

(A) let them float (B) tie them LOW **(C)**tie them HIGH (D) none

45. Why is a pull-up resistor needed for an open collector gate?

(A) to provide V_{cc} for the IC (B) to provide ground for the IC

(C) to provide the HIGH voltage (D) to provide the LOW voltage

46. The high input impedance of MOSFETs:

(A)allows faster switching **(B)** reduces input current and power dissipation

(C)prevents dense packing (D) creates low-noise reactions

47. The time needed for an output to change from the result of an input change is known as:

(A) noise immunity (B) fan-out **(C)** propagation delay (D) rise time

48. What is the advantage of using low-power Schottky (LS) over standard TTL logic?

(A)more power dissipation **(B)**less power dissipation

(C) cost is less (D) cost is more

49. Which family of devices has the characteristic of preventing saturation during operation?

(A) TTL (B) MOS **(C)** ECL (D) IIL

50._____ TTL contains active pull up in the circuit.

(A) Open collector **(B)** Totem pole (C) both (D) none

51. Fastest of the saturated logic families is

(A) ECL **(B)** TTL (C) CMOS (D) none

Chapter 3: Combinational Logic Circuits

1. The number of control lines for a 8 – to – 1 multiplexer is

   (A) 2 **(B)** 3 (C) 4 (D) 5

2. The correction to be applied in BCD adder to the generated sum is

   (A) 0101 **(B)** 0110 (C) 1101 (D) 1010

3. The gates required to build a half adder are

   (A) EX-OR gate and NOR gate **(B)** EX-OR gate and OR gate

   (C) EX-OR gate and AND gate (D) Four NAND gates

4. The device which changes from serial data to parallel data is

   (A) Counter (B) Multiplexer **(C)** Demultiplexer (D) Flip-Flop

5. A device which converts BCD to Seven Segment code is called

   (A) Encoder **(B)** Decoder (C) Multiplexer (D) Demultiplexer

6. How many select lines will a 16 to 1 multiplexer will have

   (A) 4 (B) 3 (C) 5 (D) 1

7. When the set of input data to an even parity generator is 0111, the output will be

   (A) 1 (B) 0 (C) Unpredictable (D) Depends on the previous input

8. A full adder logic circuit will have

   (A) Two inputs and one output (B) Three inputs and three outputs

   (C) Two inputs and two outputs **(D)**Three inputs and two outputs

9. How many select lines will a 32:1 multiplexer will have

   (A)5 (B) 8 (C) 9 (D) 11

10. The number of select lines m, required to select one out of n input lines is

    (A) $m = \log_2 n$ (B) $m = \log_2(n+1)$ (C)$m = \ln n$ (D) $m = 2^n$

11. The minimum number of 2-input NAND gates required to realize a half-subtractor is

    (A) 3 **(B)** 4 (C) 6 (D) 2

12. Which logic device is called a distributor?

    (A) multiplexer **(B)**demultiplexer (C) encoder (D) decoder

13. BCD subtraction is performed by using

(A) 1's complement (B) 2's complement

(C) 9's complement (D) 5's complement

14. In which of the following adder circuits is the carry ripple delay eliminated?

(A) half-adder (B) full-adder (C) parallel adder **(D)** carry look ahead adder

15. How many full-adders are required to construct an m-bit parallel adder?

(A) $m/2$ (B) $m-1$ (**C**)m (D) $m+1$

16. What device will perform the conversion of a 4 bit BCD code to seven segment code required to drive a LED read out.

(A) Decoder **(B)** BCD to Decimal decoder (C) Multiplexer (D) None

17. A circuit which gates one input of data line to one of 2^n output lines is defined as a

(A) MUX **(B)** DeMUX (C) Encoder (D) Decoder

18. A magnitude comparator 7485 outputs depend on cascading inputs only when

(A) comparing inputs are not equal **(B)** comparing inputs are equal

(C) Both (A) & (B) (D) None

19. A carry look ahead adder is frequently used for addition, because it

(A) is faster (B) is more accurate (C) uses fewer gates (D) costs less

20. A combinational circuit is one in which the output depends on the

(A) input combination at that time (B) previous output and input

(C) present output and the previous output (D) None

21. The number of full adders required to add two 4 – bit numbers in a serial adder

(A) 1 (B) 4 (C) 2 (D) 5

22.3 – to – 8 line decoder is also called

(A) one of 16 decoder **(B)** binary to octal converter (C) Both (D) None

23.Multiplexer can be implemented with

(A) OR – AND **(B)** AND – OR (C) NAND – OR (D) NOR – AND

24. How many outputs are on a BCD decoder?

(A) 4 (B) 16 (C) 8 **(D)** 10

25. What is the function of an enable input on a multiplexer chip?

(A) to apply V_{cc} (B) to connect ground

(C)to active the entire chip (D) to active one half of the chip

Chapter 4: Sequential Logic Circuits

1. A mod 5 synchronous counter is designed using JK flip-flops. The number of counts it will skip is

   (A) 2 **(B)** 3 (C) 5 (D) 10

2. A 4-bit synchronous counter uses flip-flops with propagation delay time of 25 ns each. The maximum possible time required for change of state will be

   (A) 25 ns (B) 50 ns (C) 75 ns (D) 100 ns

3. In a 4 bit ripple counter, for every input clock pulse

   (A) all the flip-flops get clocked simultaneously

   (B) only one flip-flop gets clocked at a time

   (C) two of the flip-flops get clocked at a time

   (D) all the above statements are false

4. A universal shift register

   a) accepts serial input (B) accepts parallel input

   (C) gives serial and parallel outputs **(D)** is capable of all of the above

5. The maximum number that can be obtained by a ripple counter using five flip-flops is

   a) 32 (B) 15 (C) 7 **(D)** 31

6. The number of flip-flops required for a mod-12 Johnson counter is

   a) 4 **(B)** 6 (C) 15 (D) 24

7. The output frequency of a mod 12 counter is 6 KHz. Its input frequency is

   a) 6 KHz (B) 500 Hz (C) 24 KHz **(D)** 72 KHz

8. The minimum number of flip-flops required for a mod-12 counter is

   (A) 3 **(B)**4 (C)6 (D) 12

9. A bidirectional shift register works as

   (A) left shift (B) right shift **(C)** both (D) none

10. To generate a sequence of length S , the condition to identify the number of flip-flops is

    (A) $S \leq 2^N - 1$ (B) $S \geq 2^N - 1$ (C) $S > 2^N + 1$ (D) None

11. The following sequential circuit is self-starting

(A) Ring counter **(B)** Johnson counter (C) Both (D) None

12. The characteristic equation of JK flip-flop is

(A) $Q_{n+1} = JQ_n + KQ_n$ (**B**) $Q_{n+1} = JQ_n' + K'Q_n$ (C) $Q_{n+1} = J'Q_n' + K'Q_n$ (D) None

13. Johnson counter is also known as

(A) Twisted ring counter (B) Switch tail ring counter **(C)** both (D) none

14. A synchronous counter will have

(A) high propagation delay **(B)** low propagation delay (C) both (D) none

15. The number of flip-flops required for a mod-12 Ring counter is

(A) 4 **(B)** 12 (C) 15 (D) 24

16. The minimum number of flip-flops required for a mod-8 counter is

(A) 3 (B) 4 (C) 6 (D) 12

17. Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz.

(A) 10.24 kHz **(B)**5 kHz (C) 30.24 kHz (D) 15 kHz

18. Which statement BEST describes the operation of a negative-edge-triggered D flip-flop?

(A) The logic level at the *D* input is transferred to *Q* on NGT of *CLK*.

(B) The *Q* output is ALWAYS identical to the *CLK* input if the *D* input is HIGH.

(C) The *Q* output is ALWAYS identical to the *D* input when *CLK* = PGT.

(D) The *Q* output is ALWAYS identical to the *D* input.

19. How is a *J-K* flip-flop made to toggle?

(A) *J* = 0, *K* = 0 (B) *J* = 1, *K* = 0 (C) *J* = 0, *K* = 1 **(D)** *J* = 1, *K* = 1

20. Which of the following is correct for a gated *D* flip-flop?

(A) The output toggles if one of the inputs is held HIGH.

(B) Only one of the inputs can be HIGH at a time.

(C) The output complement follows the input when enabled.

(D) *Q* output follows the input *D* when the enable is HIGH.

21. A J-K flip-flop is in a "no change" condition when _____.

(A)J = 1, K = 1 (B) J = 1, K = 0 (C) J = 0, K = 1 **(D)** J = 0, K = 0

22. What is the significance of the S and Rterminals in the SR flip-flop?

(A) There is no known significance in their designations.

(B) The *S* represents "Set," and R represents “Reset”

(C) The letters were chosen in honor of Jack Kilby, the inventory of the integrated circuit.

(D) All of the other letters of the alphabet are already in use.

23. If both inputs of an S-R flip-flop are low, what will happen when the clock goes HIGH?

(A) An invalid state will exist. **(B)** No change will occur in the output.

(C) The output will toggle. (D) The output will reset.

24. How many flip-flops are required to make a MOD-32 binary counter?

(A) 3 (B) 45 **(C)** 5 (D) 6

25. When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.

(A) product (B) sum (C) log (D) reciprocal

26. A MOD-12 and a MOD-10 counter are cascaded. Determine the output frequency if the input clock frequency is 60 MHz.

(A)5000 kHz (B)1,500 kHz (C) 6 MHz **(D)** 500 KHz

27. To operate correctly, starting a ring counter requires:

(A)clearing one flip-flop and presetting all the others.

(B) clearing all the flip-flops. (C) presetting all the flip-flops.

(D)presetting one flip-flop and clearing all the others.

28. Which of the following is an invalid output state for an 8421 BCD counter?

(**A**) 1111 (B) 0000 (C) 0010 (D) 0001

29. A 4-bit up/down binary counter is in the DOWN mode and in the 1100 state. To what state does the counter go on the next clock pulse?

(A) 1011 (B) 0000 (C) 1111 (D) 1101

30. Synchronous (parallel) counters eliminate the delay problems encountered with asynchronous (ripple) counters because the:

(A)input clock pulses are applied only to the first and last stages.

(B)input clock pulses are applied only to the last stage.

(C)input clock pulses are applied simultaneously to each stage.

(D)input clock pulses are not used to activate any of the counter stages.

31. Why can a synchronous counter operate at a higher frequency than a ripple counter?

(A)The flip-flops change one after the other.

(B) The flip-flops change at the same time.

(C)A synchronous counter cannot operate at higher frequencies.

(D)A ripple counter is faster.

32. Which of the following is a type of shift register counter?

(A) Decade **(B)** Johnson (C) Binary (D) BCD

33. Hazards may occur in _____ sequential circuits.

(A) asynchronous (B) synchronous (C) both (D)none

34. An asynchronous sequential circuit consisting of a NAND latch and OR-AND combinational circuit is _____.

(A) hazard free (B) fault free (C) both (D) none

35. Essential hazard causes _____ of an asynchronous sequential circuit.

(A) Malfunctioning (B) better working (C) both (D) none

36. In asynchronous sequential circuit, critical race must be _____.

(A) Neglected (B) considered **(C)** avoided (D) none

37. A minimum number of _____ changes must occur in the output corresponding to dynamic hazard.

(A) three (B) four (C) five (D) one

38. The number of inputs which can change simultaneously in a fundamental mode asynchronous circuit is

(A) two **(B)** one (C) three (D) four

39. Race condition may exist in _____sequential circuits.

(A) Synchronous (B) Asynchronous (C) both (D) none

40.A minimum of _____ paths must exist between an input variable and output for dynamic hazard to occur.

(A) three (B) one (C) two (D) four

Chapter 5: Memory Devices & PLDs

1.The difference between a PLA and a PAL is:

(A) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane.

(B) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane.

(C) The PAL has more possible product terms than the PLA.

(D) PALs and PLAs are the same thing.

2. PALs tend to execute _____ logic.

(A) SAP **(B)** SOP (C) PLA (D) POS

3. What does a dot mean when placed on a PLD circuit diagram?

(A) A point that is programmable **(B)** A point that cannot change

(C) An intersection of logic blocks (D) An input or output point

4. Which of the following is not a programmable device?

(A) EPROM (B) FLASH (C) FPGA **(D)** None

5. Inside any memory device, the external address lines are directly connected with

(A) decoder (B) data buffer (C)memory (D) multiplexer

6. With m address lines, how many memory locations can be addressed directly?

(A) m (B) 2m (C)4m **(D)** 2^m

7. The storage cell of DRAM is made of

(A) capacitor (B) resistor (C) BJT (D) none

8.The maximum addressable memory space with 12 address lines are

(A) 12 K (B) 36 K (C) 1.2 K **(D)** none

9. ROM is a semi conductor memory device which is

(A) volatile **(B)** non volatile (C) both (D) none

10. RAM is a semi conductor memory device which is

(A) volatile (B) non volatile (C) both (D) none

11. Information is stored in _____ form in memory chips.

(A) octal **(B)** binary (C) BCD (D) none

12. The maximum number of bytes that can be stored in a memory of size 1024 x 8 is

(A) 2048 (B) 512 **(C)** 1024 (D) 8

13. The data rate of a synchronous SRAM operating at 200 MHz is _____ .

(A) 200 MHz **(B)** 400 MHz (C) 100 MHz (D) None

14. An EPROM is erased by

(A) UV light (B) sun light (C) both (D) none

15.The number of address lines required in a memory of 128 K x 8 is

(A) 17 (B) 128 (C) 8 (D) 16

16. For designing a digital logic circuit of 32 variables, ____ PLAs with 16 inputs and 8 outputs are required.

(A) Two (B) Eight (C) Nine (D) One

17. Input buffers in PLA and PAL devices have _____ outputs.

(A) Inverting (B) Non inverting **(C)** both (D) none

18. A PLA is comprised of programmable _____ arrays.

(A) OR (B) Ex-OR **(C)** AND and OR (D) None

19. The basic storage cell of a static RAM is

(A) latch (B) transistor (C) capacitor (D) none

Chapter 6

ASM Charts

1. An ASM chart can be represented as a

   (A) state equation (**B)** state diagram (C) both (D) none

2. In an ASM chart, Mealy type of outputs

   (A) can be represented in the decision box (B) cannot be represented

   (C) can be represented by conditional output box (D) none

3. A synchronous sequential circuit can be represented using

   (A) state equation (B) state diagram (C) ASM chart (**D)** all of the above

4. An ASM chart can be implemented using

   (A)flip-flops and multiplexers (B) demultiplexers (C) adders (D) none

5. A decision box in an ASM chart

   (A) does not have exit paths (B) has only one exit path

   (**C)** has two exit paths (D) has one entry and one exit path

6. An ASM chart of the Moore model contains

   (A) outputs mentioned inside state box (B) unconditional output box

   (C) both (D) none

7. A row in the state table is the same as ____ in an ASM chart.

   (A)state box (B) decision box (C) conditional box (D) none

8. An ASM chart is the same as

   (A) synchronous sequential circuit (B) clocked sequential circuit

   (C) finite state machine **(D)** all of the above

9. A state box in an ASM chart

   (A) is not included in any ASM block

   (B) may be shared by two ASM blocks

   (C) is included in only one ASM block

   (D) may be included in any number of ASM blocks

10. ASM charts represents

    (A) gates (B) multiplexers (**C)** synchronous sequential circuits (D) none