WITH EFFECT FROM THE ACADEMIC YEAR 2008-2009

BIT 383

MINI PROJECT - IV

Instruction 3 Periods per week
Sessional 25 Marks

The students are required to carryout Mini Project in any of the areas such as Computer Networks, Object Oriented System Development.

Students are required to submit a report on the Mini Project at the end of the Semester.

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WITH EFFECT FROM THE ACADEMIC YEAR 2009-2010

SCHEME OF INSTRUCTION AND EXAMINATION

B.E. IV/IV (REGULAR)

INFORMATION TECHNOLOGY

SEMESTER - I

Sl. No.	Syllabus Ref. No.	Subject	Scheme of Instructions		Scheme of Examination		
			Periods per Week		Duration in Hrs	Maximum Marks	
			L/T	D/P		Univ. Exam	Sessionals
		THEORY					
1.	BIT 401	VLSI Design	4	-	3	75	25
2.	BIT 402	Wireless and Mobile Communications	4	-	3	75	25
3.	BIT 403	Middleware Technologies	4	-	3	75	25
4.		ELECTIVE – II	4	-	3	75	25
5.		ELECTIVE - III	4	-	3	75	25
		PRACTICALS					
1.	BIT 431	VLSI Design Lab	-	3	3	50	25
2.	BIT 432	Middleware Technologies Lab	-	3	3	50	25
3.	BIT 433	Project Seminar	-	3	-	-	25
		Total	**20**	**9**	**24**	**475**	**200**

Elective – II

BIT 404	Digital Instrumentation and Control
BIT 405	Grid Computing
BIT 406	Data Warehousing and Data Mining
BIT 407	Intellectual Property Rights

Elective – III

BIT 408	Digital Image Processing
BIT 409	CPLD & FPDA Architectures
BIT 410	Information Security
BIT 411	Software Reuse Techniques

BIT 401

VLSI DESIGN

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

UNIT-I

An overview of VLSI, Moore's law, Electrical Conduction in Silicon, Electrical Characteristics of MOSFETs Theshold voltage, nFET Current-Voltage equations, square law and linear model of a FET, MOS capacitances, gate-source and gate drain capacitances, junction capacitances in a MOSFET, RC model of a FET, modeling small MOSFET, scaling. MOSFET as switches, pass characteristics, logic gates using CMOS, Bubble pushing, XOR and XNOR gates, AOI and OAI logic gates, transmission gates. TG based 2-to-1 MUX, XOR, XNOR, OR circuits.

UNIT-II

Physical structure of CMOS ICs, IC layers, layers used to create a MOSFET, Top and side view of MOSFETs, Silicon patterning or layouts for series and parallel connected FETs. Layouts of NOT gate, transmission gate, noninverting buffer, NAND2, NOR2, Complex logic gate, 4 input AOI gate. Stick diagram representations. Layouts of Basic Structure: nwells, active area definition, design of n^+, p^+ regions, masks for the nFET, active contact cross section and mask set, metal1 line with active contact, poly contact: cross section and layout, vias and higher level metals. Latchup prevention.

UNIT-III

Fabrication of CMOS ICs, CMOS process flow, Design rules: minimum space width, minimum spacing, surround, extension, cell concepts and cell based design, logic gates as basic cells, creation of new cell using basic gates. DC characteristics of the CMOS inverter symmetrical inverter, layouts, Inverter switching characteristics, RC switch model equivalent for the CMOS inverter, fanout, input capacitance and load effects, rise time and fall time calculation, propagation delay, driving large capacitive loads, delay minimization in an inverter cascade.

UNIT-IV

Pseudo nMOS, tristate inverter circuits, chocked CMOS, charge leakage, Dynamic CMOS logic circuits, precharge and evaluation charge sharing, Domino logic, Dual rail logic networks, differential Cascade Voltage Switch Logic (CVSL) AND/NAND, OR/NOR gates, Complementary Pars Transister Logic (CPL). The SRAM, 6T SRAM cell design parameters, writing to an SRAM, resistor model, SRAM cell layout, multi port SRAM, SRAM arrays, Dynamic RAMs: 1T RAM cell, charge leakage and refresh in a DRAM cell, physical design of DRAM cells. NOR based ROM, ROM array using pseudo nMOS circuitry, floating gate MOSFET, effect of charge storage on the floating gate, A E^2PROM word using floating gate nFETs, logic gate diagram of the PLA, NOR based design, CMOS PLA, Gate arrays, gate array base.

UNIT-V

VLSI Design flow, structural gate level modeling, gate primitives, gate delays, switch level modeling, behavioral and RTL operators, timing controls, blocking and non blocking assignments, conditional statements, Data flow modeling and RTL, Comparator and priority encoder barrel shifter, D latch Master slave D type flip-flop, Arithmetic circuits: half adder, full adder, AOI based, TG based, ripple carry adders, carry look ahead adders, High speed adders, multipliers. Interconnect modeling; Interconnect resistance and capacitance sheet resistance Rs, time delay, single and multiple rung ladder circuits, simple RC inter connect model, modeling inter connect lines with a series pass FET, cross talk, floor planning and routing, clocking, Testing of VLSI circuits.

Suggested Reading:

1. John P. Uyemura, *"Introduction to VLSI circuits and Systems"*, John Wiley & Sons, 2002

Reference:

1. John P. Uyemura, *"Chip design for submicron VLSI: CMOS layout and simulation"* IE (a part of cengage learning) 2006.
2. Douglas A. Pucknell, Kamran Eshraghian, *"Basic VLSI Design"* 3rd Edition, PHI, 2000.
3. Jan M. Rabey and others *"Digital Integrated Circuits A design perspective"*, Pearson Education

BIT 402

WIRELESS AND MOBILE COMMUNICATION

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

UNIT –I

Introduction to Wireless Communication Systems: Evolution of Mobile Radio Communications, Examples of Wireless Communication Systems. Modern Wireless Communication Systems : Second Generation (2G) Cellular Networks, Third Generation (3G) Wireless Networks, Wireless local Loop, Wireless Local Area Networks. Concepts of WiFi, WimMax The Cellular Concept: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies, Interference and Systems Capacity, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems.

UNIT –II

Mobile Radio Propagation : Large Scale - :Path Loss : Introduction to Radio Wave Propagation, Free Space Propagation Model, Three Basic Propagation Mechanisms, Reflection, Ground Reflection, Diffraction, Scattering, Outdoor Propagation Models, Indoor Propagation Models, Signal Penetration into Buildings.

UNIT –III

Modulation Techniques for Mobile Radio : Digital Modulation, Linear Modulation Techniques, Constant Envelop Modulation, Spread Spectrum Modulation Techniques.

UNIT –IV

Multiple Access Techniques for Wireless Communications : FDMA, TDMA, Spread Spectrum Multiple Access, Space Division Multiple Access, Capacity of Cellular Systems. Wireless Networking :

Introduction, Difference between Wireless and Fixed Telephone Networks, Development of Wireless Networks. Wireless Systems and Standards: Global System for Mobile (GSM), GPRS, CDMA Digital Cellular Standard.

UNIT –V

Mobile Network Layer: Mobile IP : Goals & Requirements, Terminology, IP Packet Delivery, Agent Advertisement & Discovery, Registration, Tunneling and Encapsulation, Optimizations, Reverse Tunneling. Dynamic Host Configuration protocol.Mobile Transport Layer: Traditional TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast Recovery, Transmission/Time-Out Freezing, Selective retransmission, Transaction oriented TCP.

Suggested Reading:

1. Theodore S. Rappaport, "*Wireless Communications Principle and Practice* ", 2nd Edition, Pearson Education, 2003.
2. Jochen Schiller, *"Mobile Communication"*, 2nd Edition, Pearson Education, 2008.

BIT 403

MIDDLEWARE TECHNOLOGIES

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Client/Server Concepts: Client – Server – File Server, Database server, Group server, Object server, Web server. Middleware – General middleware – Service specific middleware. Client/Server Building blocks – RPC – Messaging – Peer – to – Peer. Web Services- SOA, SOAP, WSDL, REST Services

UNIT-II

Servlets: Servlet Lifecycle, sending HTML information, Session tracking, JDBC API, Applications. Struts: An introduction to Struts Framework, Basic components of struts, Model Layer, view Layer, Controller Layer, and Validator.

UNIT-III

EJB Architecture: EJB –EJB Architecture – Overview of EJB software architecture – View of EJB – Conversation – Building and Deploying EJBs – Roles in EJB. EJB Applications: EJB Session Beans – EJB entity beans – EJB clients – EJB Deployment – Building an application with EJB.

UNIT-IV

CORBA: CORBA – Distributed Systems – Purpose – Exploring CORBA alternatives – Architecture overview – CORBA and networking model – CORBA object model – IDL – ORB – Building an application with CORBA.

UNIT-V

COM: COM – Data types – Interfaces – Proxy and stub – Marshalling – Implementing server/Client – Interface pointers – Object Creation, Invocation, Destruction – Comparison COM and CORBA – Introduction to .NET – Overview of .NET architecture–Marshalling – Remoting

Suggested Reading:

1. Robert Orfali, Dan Harkey and Jeri Edwards, "The Essential Client/ server Survival Guide" . Galgotia publications Pvt. Ltd., 2002.(Unit 1)
2. Tom Valesky, "Enterprise Java Beans", Pearson Education, 2002. (Unit 2 & 3)
3. Jason Pritchard. "COM and CORBA side by side", Addison Wesley, 2000 (Unit 4 & 5)
4. Jesse Liberty, "Programming C#", 2nd Edition, O'Reilly press,2002. (Unit 5)
5. Arno Puder, kay Romere and Frank pilhofer. Distributed Systems Architecture, Morgan Kaufman 2006
6. Struts: the complete reference By James Holmes Edition: 2, illustrated Published by McGraw-Hill Professional, 2006(added)(unit-2)
7. Java Servlet Programming By Jason Hunter, William Crawford Edition: 2, illustrated Published by O'Reilly, 2001(unit-2)(added)

Reference:

1. Mowbray, " Inside CORBA", Pearson Education, 2002.
2. Jeremy Rosenberger, "Teach yourself CORBA in 14 days", Tec media, 2000

3IT 404

DIGITAL INSTRUMENTATION & CONTROL
(Elective - II)

nstruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT –I

Introduction to process control Introduction, control systems, process control block diagram, control system evaluation, time response, significance and statistics. Analog signal conditioning. principles of analog signal conditioning, passive circuits, op amps, op-amps in instrumentation, Industrial Electronics. Digital Signal Conditioning: Review of digital fundamentals, comparators, DAC's ADC's data acquisition systems (DAS)

UNIT – II

Thermal Sensors: Metal resistance Vs temperature devices, thermistors, thermocouples, bimetal strips, Gas thermometer, vapor pressure thermometer, liquid expansion thermometer, solid state temperature sensors.Mechanical Sensors displacement, location or position sensors, strain sensors, motion sensors, pressure sensors, flow sensors.

UNIT –III

Optical Sensors : Fundamentals of EM radiation, photo detectors, pyrometry, optical sources, applications. Final control : Final Control operation, signal conversions, actuators, control elements.

UNIT – IV

Desecrate – state process control : Definition , characteristics of the system, ladder diagram, Programmable logic controllers. Controller principles : Process characteristics, control system parameters, discontinuous, continuous and composite controller modes.

UNIT – V

Analog controllers: Electronic controllers, pneumatic controllers, design considerations. Digital Controllers Digital electronics methods, computers in process control, characteristics of digital data, controller software.Control loop characteristics: Control system configurations, multivariable control systems, control system quality, stability, process loop tuning.

Suggested Reading:

1. Curtis Johnson, "Process Control Instrumentation Technology", 4th Edition, PHI-2001 .
2. W Bolton , Mechatronics, "Electronic Control Systems in Mechanical and Electrical Engineering". 2nd Edition, Pearson Education, Asia, 2001.
3. CS Rangan, G.R. Sarma, V.S.V Mani, "Instrumentatin Devices & Systems" 2nd Edition. Tata McGraw Hill,2002.

BIT 405

GRID COMPUTING
(Elective - II)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction to High Performance Computing: Early Grid Activities, Current Grid Activities, Grid Business Areas, Grid Applications. Grid Computing Organizations and Their Roles: Developing Grid Standards & Best Practice Guidelines, Developing Grid Computing Toolkits & Frameworks, Grid-Based Solutions to Solve Computing, Data, and Network Requirements, Building and Using Grid-Based Solutions Commercially.

UNIT-II

Grid Computing Anatomy: The Grid Problem, The Grid Computing Roadmap, Grid Services Architecture and Web Services Architecture.

UNIT-III

OGSA: Introduction, Sample Use Cases that Drive the OGSA, OGSA Platform Components, Open Grid Services Infrastructure (OGSI), OGSA Basic Services.

UNIT-IV

The Grid Development Toolkits: Globus GT3 Toolkit: Architecture, Globus GT3 Toolkit: Programming Model, Globus GT3 Toolkit: Implementation Globus GT3 Toolkit: High-Level Services.

UNIT-V

Message Passing Interface (MPI) Standard: Overview, Procedures and Arguments, Data Types, Processes, Error Handling, Platform

Independence, Point-to-Point Communication, Collective Communication, Groups – Contexts – Communicators, Process Technologies.

Suggested Reading:

1. Joshy Joseph, Craig Fellenstein – Grid Computing, Pearson Education, 2004.
2. Vladimir Silva – Grid Computing for Developers, Dreamtech Press, 2006.

Reference:

1. Ahmar Abbas – Grid Computing – A Practical Guide to Technology and Applications, Firewall Media, 2006.

BIT 406

DATA WAREHOUSING AND DATA MINING
(Elective - II)

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

UNIT – I

Introduction: What is Data Mining, Data Mining Functionalities, Classification of Data Mining Systems, Major Issues in Data Mining.Data Preprocessing: Needs Preprocessing, Descriptive Data Summarization, Data Cleaning, Data Integration and Transformation, Data Reduction, Data Discretization and Concept Hierarchy Generation.

UNIT – II

Data Warehouse and OLAP Technology: What is Data Warehouse, A Multidimensional Data Model, Data Warehouse Architecture and Implementation, from Data Warehousing to Data Mining.
Mining Frequent Patterns, Associations Rules: Basic Concepts, Efficient and Scalable Frequent Item Set Mining Methods, Mining Various kinds of Association Rules.

UNIT – III

Classification and Prediction: Introduction, Issues Regarding Classification and Prediction, Classification by Decision Tree Induction, Bayesian Classification, Rule based Classification, Classification by Back Propagation, Support Vector Machines, Prediction, Accuracy and Error Measures

UNIT – IV

Cluster Analysis: Introduction, Types of Data in Cluster Analysis, A Categorization of Major Clustering Methods, Partitioning Methods, Hierarchical Methods, Density-Based Methods, Grid Based Methods, Model Based Clustering Methods, Outlier Analysis

UNIT – V

Mining Object, Spatial, Multimedia, Text, and Web Data: Multidimensional Analysis and Descriptive Mining of Complex Data Objects, Spatial Data Mining, Multimedia Data Mining, Text Mining, Mining the World Wide Web.

Suggested Reading:

1) Han J & Kamber M, "Data Mining: Concepts and Techniques", Harcourt India, Elsevier India, Second Edition.
2) Pang-Ning Tan, Michael Steinback, Vipin Kumar, "Introduction to Data Mining", Pearson Education, 2008.

Reference:

1) Margaret H Dunham, S.Sridhar, "Data mining: Introductory and Advanced Topics", Pearson Education, 2008.
2) Humphires, Hawkins, Dy, "Data Warehousing: Architecture and Implementation", Pearson Education, 2009.
3) Anahory, Murray, "Data Warehousing in the Real World", Pearson Education, 2008.
4) Kargupta, Joshi,etc., "Data Mining: Next Generation Challenges and Future Directions" Prentice Hall of India Pvt Ltd, 2007.

BIT 407

INTELLECTUAL PROPERTY RIGHTS
(Elective - II)

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

UNIT –I

Introduction : Meaning of Intellectual Property- Nature of I.P- Protection of I.P. Rights-kinds of Intellectual Property Rights –International Conventions of Intellectual Property Rights- patent Traty 1970, GATT 1994, TRIPS & TRIMS – International Organization for Protection of IPR – WTO, WIPRO, UNESCO.

UNIT –II

Patents: Meaning of Patent- Commercial Significance – Obtaining of Patent – patentable Subject – matter – rights and obligations of Patentee – specification – Registration of patents – Compulsory licensing and licenses of rights – Revocation.

UNIT –III

Industrial Designs : Definitions of Designs – Registration of Designs – Rights and Duties of Proprietor of Design – Piracy of Registered Designs.

UNIT –IV

Trade Marks : Meaning of trademark – purpose of protecting trademarks Registered trade mark – procedure – passing off – Assignment and licensing of trade marks – Infringement of trademarks.

UNIT – V

Nature, scope of copyright – Subject matter of copy right – Right conferred by copyright- Publication – Broad – casting, telecasting – computer programme – Database right – Assignment – Transmission of copyright – Infringement of copy right.

Suggested Reading :

1. Cornish W.R, "Intellectual Property Patents", Copyright, Trademarks and Allied Rights, Sweet & Maxwell 1993.
2. P . Narayanan, " Intellectual Property Law ", Eastern law House 2nd Edn. 1997.
3. Robin Jacob & Daniel Alexander, " A Guide Book to Intellectual Property Patents, Trademarks, Copy rights and designs, Sweet and Maxwell, 4th Edn.,1993.

BIT 408

DIGITAL IMAGE PROCESSING
(Elective - III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Image processing: Introduction, Fundamental steps, Components. Elements of visual perception, image sampling and quantization, some basic relationships between pixels. Intensity Transformations: Some Basic Intensity Transformation Functions, Histogram Processing

UNIT-II

Spatial Filtering: Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters Filtering in the Frequency Domain: Preliminary Concepts, Image Smoothing using Frequency Domain Filters, Image Sharpening Using Frequency Domain Filters.

UNIT-III

Image Restoration and Reconstruction : A Model of the Image degradation/Restoration Process, Noise Models, Restoration in the Presence of Noise Only—Spatial Filtering, Minimum Mean Square Error (Wiener) Filtering Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing

UNIT-IV

Image Segmentation: Fundamentals, Point, Line, and Edge Detection, Segmentation by Thresholding, Region-Based Segmentation. Representation and Description: Representation, Some Simple Descriptors, Shape Numbers, Fourier Descriptors. Object Recognition: Patterns and Pattern Classes, Matching: Minimum distance classifier, correlation.

UNIT-V

Color Image Processing: Color Fundamentals, Color Models, Pseudo color Image Processing. Image Compression: Fundamentals, Huffman Coding, LZW Coding.

Suggested Reading:

1) Rafael C Gonzalez and Richard E Woods, "Digital Image Processing", Pearson Education, 3nd Edition.

References:

1) Milan Sonka, Vaclav Halvac and Roger Boyle, "Image Processing, Analysis, and Machine Vision", Second Edition, Thomson Learning Publishers.
2) Kenneth R.Castleman, "Digital Image Processing", Pearson Education.
3) Rapel C Gonzalez , Richard E Woods and Steven L Eddins, "Digital Image Processing using MATLAB", Pearson Education.
4) Madhuri A Joshi, "Digital Image Processing: An Algorithmic Approach", PHI Learning Pvt Ltd, 2008.
5) S. Annadurai, R. Shanmuga Lakshmi, "Fundamental of Digital Image Processing", Pearson Education.

BIT 409

CPLD & FPGA ARCHITECTURES
(Elective - III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT – I

Programmable Logic Devices: Introduction, PROM, EPROM, EEPROM, PLE, Combinational logic design using PLEs, Sequential Circuit realization using PLEs, Signetics corporation Field Programmable Logic Array (FPLA) devices, Organization of Series-28 sequencers, series-20 sequencers, Series-24 sequencer family, Application of FPLS devices.

UNIT – II

Programmable Array Logic (PAL): Combinational, sequential and arithmetic PAL devices, PAL series 24, PAL 23s8, Mega PALs, Hard Array Logic (HAL). New generation of PLD: Erasable PLDs, Reprogrammable Generic Logic Devices, Erasable Programmable Logic Array (EPLA), Generic Array Logic (GAL), Programmable Electrically Erasable Logic (PEEL) devices, PAL29M16, PLDs with foldback architecture, PML, ERASIC, Programmable state machines, Programmable Gate Array.

UNIT – III

FPGAs: Introduction, Programming Technologies: SRAM, Antifuse, EPROM and EEPROM Xilinx FPGAs, Actel, Altera, Plessey, Plus Logic, AMD, Quick Logic, Algotromix, Concurrent Logic FPGAs. Crosspoint Solutions FPGA, translation to XNF format, Partition, Place and route, Technology mapping for FPGAs: Logic Synthesis, logic Optimization, Lookup Table Technology Mapping, Mapping into Xilinx 3000 CLBs, Multiplexer Technology, Mapping.

UNIT – IV

Logic Block Architecture: Logic Block functionality Versus area-efficiency, Impact of Logic Block Functionality in FPGA performance, Routing for FPGAs: Segmented Channel Routing, Routing for Symmetrical FPGAs, CGE detailed router Algorithm. Flexibility of FPGA routing architectures: Logic Block, Connection Block, Trade offs in Flexibilities of the S and C blocks, A theoretical model for FPGA routing.

UNIT – V

Platform FPGA architectures, Multi-FPGA Systems: Xilinx Virtex II Pro Platform FPGA, Altera Stratix Platform FPGA, Serial I/O, Memories, CPUs and Embedded Multipliers, Multi FPGA systems: Interconnecting Multiple FPGAs, partitioning, Novel architectures.

Suggested Reading:

1. Parag K. Lala, "Digital System Design using Programmable Logic Devices", BS Publications, Reprint 2008 (Unit I & II)
2. Stephen D. Brown, Robert J Francis, Jonathan Rose, Ivonko G. Vranesic, "Field Programmable Gate Arrays", Springer International Edition, First Indian Print 2007(Unit III & IV)
3. Wayne Wolf, "FPGA-based System Design", Pearson Education, First Impression, 2009 (Unit V)

References:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology" Springer International Edition", First Indian Reprint 2007.
2. Michel John Sebastian Smith "Application – Specific Integrated Circuits", Pearson Education, First Indian reprint 2000.

BIT 410

DIGITAL IMAGE PROCESSING
(Elective - III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction: Characteristics of Information, Components of Information Systems, Securing components, balancing Security and Access The Security System Development Life Cycle, Security Professionals and the organization.Security Investigation Phase; Need for security, Threats, Attacks.

UNIT-II

Legal, Ethical, and Professional Issues in Information Security Ethical Component in Information System, Codes of Ethics, Certification Security Analysis: Risk Management, Identifying and assessing risk, Controlling Risk.

UNIT-III

Logical Design: Blue print for security. Security Policy, standards and Practices.Design of Security Architecture, Physical Design: Security Technology, Physical Design of Security SDLC Firewalls, Dialup Protection, Intrusion Detection Systems, Scanning and analysis tools, Content filters.

UNIT-IV

Cryptography: The basic elements of cryptography: symmetric (Symmetric Key-DES, IDEA, and

AES), and public key cryptography (Public Key Encryptions-RSA).

UNIT-V

Message digest (MD-5, SHA), digital signatures. SSL and SET: SSL and SET protocols, Internet transactions using both SSL and SET.

Suggested Reading:

1. Michael E. Whitman and Herbert J. Mattord, "Principles of Information Security", Thomson, 2003.
2. William Stallings, "Cryptography and Network Security", Pearson Education, 2000.
3. Nina Godbole, "Information System Security", Wiley India Pvt. Ltd.

BIT 411

SOTWARE REUSE TECHNIQUES
(Elective - III)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT – I

Software reuse success factors, Reuse driven software engineering as business, Object oriented software engineering, Applications and Component subsystems, Use case components, Object components.

UNIT – II

Design Patters – Introduction. Creational Patterns – Factory, factory method, abstract factory, singleton, builder, prototype.

UNIT – III

Structural Patterns – Adapter, bridge, composite, decorator, façade, flyweight, proxy. Behavioral Patterns – Chain of responsibility, command, interpreter.

UNIT – IV

Behavioral Patterns – Interartor, mediator, memento, observer, state, strategy, template, visitor. Other design patterns – Whole – part, master – slave, view handler, forwarder – receiver, client dispatcher – server, publisher – subscriber.

UNIT – V

Architectural Patterns – Layers, pipes and filters, black board, broker, model-view controller, presentation – abstraction – control, micro kernel, reflection.

Suggested Reading:

1. Ivar Jacabson, Martin Griss, Patrick Johnson, *"Software Reuse: Architecture, Process and Organization for Business Success"*, ACM Press 1997.
2. Erich Gamma, Richard Helm, Ralph Johnson, John Vlissides – *" Design Patterns"*, Pearson Education, 1995.
3. Frank Buschmann etc., - *"Pattern Oriented Software Architecture – Volume I"*, Wiley 1996.
4. James W Cooper, *"Java Design Patterns, a tutorial"*, Pearson Education, 2000.

BIT 431

VLSI DESIGN LAB

Instruction	3 Periods per week
Duration of University Examination	3 Hours
University Examination	50 Marks
Sessional	25 Marks

1. Switch level modeling using Verilog
   a) Logic gates b) AOI and OAI gates
   c) Transmission gate d) Complex logic gates using CMOS
2. Structural Gate-level Modeling [With and Without delays] – Digital circuits using gate primitives – using Verilog.
   a) AOI gate b) Half adder and full adders
   c) MVX using buffers d) S-R latch etc.
3. Mixed gate –level and Switch-level modeling using Verilog-usage of primitives, modules and instancing and understanding the hierarchical design.
   a) Constructing a 4-input AND gate using CMOS 2-input NAND and NOR gates.
   b) constructing a decoder using CMOS 2-input AND gates and NOT gates etc.
4. RTL Modeling of general VLSI system components.
   a) MUXes b) Decoders c) Priority encodes
   d) Flip-flops e) Registers.
5. Synthesis of Digital Circuits
   a) Ripple carry adder and carry look-ahead adder
   b) array multiplier
6. Verilog code for finite state machine
7. Modeling of MOSFET
8. Stick diagram representations. Simple layouts of Inverter. Understanding the concepts of Design Rule checking.
9. Fault Modeling for Stuck-at-O and Stuck-at-1 faults.
10. Clock generation circuits (study)

BIT 432

MIDDLE WARE TECHNOLOGIES LAB

Instruction	3 Periods per week
Duration of University Examination	3 Hours
University Examination	50 Marks
Sessional	25 Marks

1. Create a distributed name server (like DNS) RMI
2. Create a Java Bean to draw various graphical shapes and display it using or without using BDK
3. Develop an Enterprise Java Bean for student Information System.
4. Develop an Enterprise Java Bean for Library operations.
5. Create an Active-X control for Timetable.
6. Develop a component for converting the currency values using COM/ .NET
7. Develop a component for browsing CD catalogue using COM / .NET
8. Develop a component for retrieving information from message box using DCOM/NET
9. Develop a middleware component for retrieving Stock Market Exchange information using CORBA
10. Develop a middleware component for retrieving Bank Balance using CORBA

BIT 433

PROJECT SEMINAR

Instruction	3 Periods per week
Sessional	25 Marks

Oral presentation is an important aspect of engineering education. The objective of the seminar is to prepare the students for a systematic and independent study of the state of the art topics in a broad area of his / her specialization. Project Seminar serves as an aid to get acquainted thoroughly with the broad area of the student's final year project work and serves as necessary groundwork for the successful carrying out of the project work. Project seminar is to help the students to select the broad area for final year project, place of work, and to decide the approach and methodology of project work. So, Project Seminar topics need to be chosen by the students with advice and approval from the faculty members/industry personal who are going to guide their final project work. Students are to be exposed to the following aspects of a seminar presentation.

- Literature Survey
- Technical writing
- Organization of the material
- Preparation of Power Point Slides
- Power Point Slide Presentation

For award of Sessional marks, students are judged, on the basis of oral and written presentation skills as well as their involvement in the discussions, by a team comprising of at least two faculty members.

Each student is required to:

a) submit a one-page synopsis to get the approval of the topic.

b) to maintain a Project Dairy where in the progress of project work need to be recorded and signed at least once in a week by the guide(s).

c) submit Seminar Report on the approved topic at least one week ahead of the scheduled day of presentation and the report should be as per the common guidelines provided by the department along with a list of references and the set of ppt slides prepared for the presentation.

d) present seminar on approved topic for about 20 minutes using ppt slides, followed by 10 minutes discussion.

e) be present on all the days of seminar presentation and to involve actively in the technical discussions/ interactions at the end of every presentation.

Seminars are to be scheduled from the 4th week of the semester to the last week of the semester and any change in the schedule is discouraged.

WITH EFFECT FROM THE ACADEMIC YEAR 2009-2010

SCHEME OF INSTRUCTION AND EXAMINATION

B.E. IV/IV (REGULAR)

INFORMATION TECHNOLOGY

SEMESTER - II

Sl. No.	Syllabus Ref. No.	Subject	Scheme of Instructions		Scheme of Examination		
			Periods per Week		Duration in Hrs	Maximum Marks	
			L/T	D/P		Univ. Exam	Sessionals
		THEORY					
1.	BIT 451	Embedded Systems	4	-	3	75	25
2.		ELECTIVE – IV	4	-	3	75	25
3.		ELECTIVE - V	4	-	3	75	25
		PRACTICALS					
1.	BIT 481	Embedded System Lab	-	3	3	50	25
2.	BIT 482	Seminar	-	3	-	-	25
3.	BIT 483	Main Project	-	6	Viva Voce	Gr*	50
		Total	12	12	-	275	175

Elective – IV

BIT 452	Information Storage and Management
BIT 453	Information Retrieval Systems
BIT 454	Pattern Recognition
BIT 455	Advanced Microprocesors and Microcontrollers

Elective – V

BIT 456	Soft Computing
BIT 457	Human Computer Interaction
BIT 458	Software Project Management
BIT 459	Entrepreneurship

* Grade : Excellent/Very Good/Good/Satisfactory/Unsatisfactory

BIT 451

EMBEDDED SYSTEM DESIGN

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Embedded Computing: Introduction, Complex Systems and Microprocessor, Embedded System Design Process, Formalisms for System Design, Design Examples. The 8051 Architecture: Introduction, 8051 Micro controller Hardware, Input/Output Ports and Circuits, External Memory, Counter and Timers, Serial data Input/Output, Interrupts.

UNIT-II

Basic Assembly Language Programming Concepts: Assembly Language Programming Process, Programming Tools and Techniques, Programming the 8051. Data Transfer and Logical Instructions. Arithmetic Operations, Decimal Arithmetic. Jump and Call Instructions, Further Details on Interrupts.

UNIT-III

Applications: Interfacing with Keyboards, Displays, D/A and NO Conversions, Multiple Interrupts, Serial Data Communication. Introduction to Real- Time Operating Systems: Tasks and Task States, Tasks and Data, Semaphores, and Shared Data; Message Queues, Mailboxes and Pipes, Timer Functions, Events, Memory Management, Interrupt Routines in an RTOS Environment.

UNIT-IV

Basic Design Using a Real-Time Operating System: Principles, Semaphores and Queues, Hard Real-Time Scheduling Considerations, Saving Memory and Power, An example RTOS like uC-OS (Open Source); Embedded Software Development Tools: Host and Target

machines, Linker/Locators for Embedded Software, Getting Embedded Software into the Target System; Debugging Techniques: Testing on Host Machine, Using Laboratory Tools, An Example System.

UNIT-V

Introduction to advanced architectures: ARM and SHARC, Processor and memory organization and Instruction level parallelism; Net advanced embedded systems: Bus protocols, 12C bus and CAN bus; Internet-Enabled Systems, Design Example-Elevator Controller.

Suggested Reading:

1. Computers and Components, Wayne Wolt Elsevier.
2. The 8051 Microcontroller, Third Edition, Kenneth J.Ayala, Thomson.
3. An Embedded Software Primer, David E. Simon, Pearson Education

Reference:

1. Embedding system building blocks, Labrosse, via CMP publishers.
2. Embedded Systems, Raj Kamal, Tata McGraw Hill.
3. Micro Controllers, Ajay V Deshmllkhi, TMIL
4. Embedded System Design, Frank Vahid, Tony Givargis, John Wiley

BIT 452

INFORMATION STORAGE AND MANAGEMENT
(Elective - IV)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction to Storage Technology:

Review data creation and the amount of data being created and understand the value of data to a business, challenges in data storage and data management, Solutions available for data storage, Core elements of a data center infrastructure, role of each element in supporting business activities

UNIT-II

Storage Systems Architecture:

Hardware and software components of the host environment, Key protocols and concepts used by each component ,Physical and logical components of a connectivity environment ,Major physical components of a disk drive and their function, logical constructs of a physical disk, access characteristics, and performance Implications, Concept of RAID and its components , Different RAID levels and their suitability for different application environments: RAID 0, RAID 1, RAID 3, RAID 4, RAID 5, RAID 0+1, RAID 1+0, RAID 6, Compare and contrast integrated and modular storage systems ,High-level architecture and working of an intelligent storage system

UNIT-III

Introduction to Networked Storage:

Evolution of networked storage, Architecture, components, and topologies of FC-SAN, NAS, and IP-SAN , Benefits of the different networked storage options, Understand the need for long-term archiving solutions and describe how CAS fulfill the need , Understand the appropriateness of the different networked storage options for different application environments

UNIT-IV

Information Availability & Monitoring & Managing Datacenter: List reasons for planned/unplanned outages and the impact of downtime, Impact of downtime, Differentiate between business continuity (BC) and disaster recovery (DR) ,RTO and RPO, Identify single points of failure in a storage infrastructure and list solutions to mitigate these failures , Architecture of backup/recovery and the different backup/ recovery topologies , replication technologies and their role in ensuring information availability and business continuity, Remote replication technologies and their role in providing disaster recovery and business continuity capabilities. Identify key areas to monitor in a data center, Industry standards for data center monitoring and management, Key metrics to monitor for different components in a storage infrastructure, Key management tasks in a data center

Unit -V

Securing Storage and Storage Virtualization : Information security, Critical security attributes for information systems, Storage security domains, List and analyzes the common threats in each domain, Virtualization technologies, block-level and file-level virtualization technologies and processes

Case Study:

1. The technologies described in the course are reinforced with EMC examples of actual solutions.
2. Realistic case studies enable the participant to design the most appropriate solution for given sets of criteria.

Suggested Reading :

1. EMC Corporation, Information Storage and Management, Wiley, ISBN number: 04702942134.
2. Robert Spalding, "Storage Networks: The Complete Reference", Tata McGraw Hill , Osborne, 2003.
3. Marc Farley, "Building Storage Networks", Tata McGraw Hill, Osborne, 2001.
4. Meeta Gupta, Storage Area Network Fundamentals, Pearson Education Limited, 2002.

BIT 453

INFORMATION RETRIEVAL SYSTEMS
(Elective - IV)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction: Basic concepts, Past present and Future of IRS, Retrieval Process. Modeling: Introduction, A Taxonomy of IR Models, Retrieval: Adhoc and Filterig, A formal characterization of IR Models, Classic IR, Set Theoretic Models, Algebraic Models, Probabilistic Models, Structured Text Retrieval Models, Models for Browsing.

UNIT-II

Retrieval Evaluation: Introduction, Reference Collections. Query languages: Introduction, Keyword-based querying, pattern Matching, Structural Queries, Query Protocols.

UNIT-III

Query operations: Introduction, User Relevance Feedback, Automatic Local Analysis, Automatic Global Analysis. Text and Multimedia Languages and Properties: Introduction, Meta Data, Text, Markup Languages, Multimedia.

UNIT-IV

Text operations: Introduction, Document Preprocessing, Document Clustering, Text Compression, Comparing Text Compression Techniques. Indexing: Introduction, Inverted Files, Other Indices for Text Searching, Boolean Queries,

UNIT-V

Searching: Sequential Searching, Pattern Matching, Structural Queries, Compression. Parallel and Distributed IR: Introduction, Parallel IR, Distributed IR.

Suggested Reading:

1) Ricardo, Baeza-yates, Berthier Ribeiro-Neto, "Modern Information Retrieval" Pearson Education, 2008

Reference:

1) W.B. Frakes, Ricardo Baeza Yates, "Information Retrieval: Data Structures & Algorithms", Pearson Education, 2008.

2) Gerald Kowalski, "Information Retrieval Systems: Theory and Implementation", Kluwaer Academic Publishers, 1997.

BIT 454

PATTERN RECOGNITION
(Elective - IV)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT I

Machine Perception, Patter Recognition Systems, The Design Cycle, Learning and Adaptation. Bayesian Decision Theory: Introduction, Contiguous Classifications, Minimum Error Rate Classification, Zero-One Loss Function, Classifiers, Discriminant Functions, and Decision Surfaces

UNIT II

Normal Density: Univariate and Multi-Variate Density, Discriminant Functions For Normal Density, Different Cases, Bayesian Decision Theory – Discrete Features, Compound Bayesian Decision Theory and Context

UNIT III

Maximum Likelihood and Bayesin Parameter Estimation: Introduction, Maximum Likelihood Estimation, Bayesin Estimation, Bayesin Parameter Estimation- Gaussian Case, Bayesin Estimation: General Theory, Hidden Morkov Models

UNIT IV

Unsupervised Learning and Clustering: Introduction, Mixture Densities and Identifiability. Maximum Likelihood Estimates, Application to Normal Mixtures, K-Means Clustering, Date Description and Clustering, Criteria Function for Clustering, Hierarchical Clustering.

UNIT V

Component Analysis: Principle Component Analysis, Non-Linear Component Analysis, Low Dimension Representations and Multi Dimensional Scaling

Independent Component Analysis

Suggested Reading:

1. Richard O. Duda, Peter E. Hart, David G. Stroke, "pattern Classifications", Wiley student Edition, Second Edition.

Reference:

1. Robert Schalkoff, "Pattern Recognition: Statistical, Structural and Neural Approaches", Wiley student Edition.

BIT 455

ADVANCED MICROPROCESSORS & MICROCONTROLLERS
(Elective - IV)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

80386 Micro Processors: Review of 8086, Salient features of 80386, Architecture and Signal Description of 80386, Register Organization of 80386, Addressing Modes, Data Types of 80386, Real Address mode of 80386, Protected mode of 80386, Segmentation Paging, Virtual 8086 Mode, Enhanced Instruction set of 80386, the Co-processor 80387.

UNIT-II

Pentium 4: Salient features of Pentium 4, Instruction Translation for Pentium 4, Instruction Translation Look aside Buffer and Branch Prediction, Rapid Execution Module, Memory Subsystem, Hyper threading Technology Hyper threading in Pentium, Extended Instruction set in Advanced Pentium Processors, Instruction Set.

UNIT-III

PIC Microcontroller: Introduction, Architectural Overview, Memory Organization, Data Memory and Flash Memory, Interrupts and Reset, I/O Ports, Timer, Analog to Digital I/O.

UNIT-IV

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts and Vector Table, Architecture Revisions, ARM Processor Families, ARM Instruction Set, Thumb Instruction Set.

UNIT-V

Exception and Interrupt Handling - Exception Handling, Interrupts, Interrupt Handling schemes, Firmware, Embedded Operating Systems, Caches-Cache Architecture, Cache Policy, Introduction to DSP on the ARM , DSP on the ARM7TDMI, ARM9TDMI, Strong ARM, ARM9E, ARM10E

Suggested Reading:

1. A.K. Ray, K.M. Bhurchandi "Advanced Microprocessors and Peripherals", 2nd Edition, Tata McGrawHill, 2006.(For Unit I,II)
2. Barnett, Cox&O'Cull "Embedded C Programming and the Microchip PIC" Thomson India Edition, 2007.(For Unit III)
3. Andrew N. Sloss, Donimic Symes, Chris Wright, "ARM System Developer's Guide", Elsevier,2007.(For Unit IV,V)

Reference:

1. Steve Heath "Embedded Systems Design", 2nd Edition, Elsevier, 2008.
2. Arnold S. Berger, " Embedded Systems Design-An Introduction to Processes, Tools, & Techniques", CMP Books, 2005.

BIT 456

SOFT COMPUTING
(Elective - V)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT-I

Introduction: Neural networks, application scope of neural networks, fuzzy logic, genetic algorithm, hybrid systems, Soft computing. Artificial neural networks: Fundamental concepts, Evolution of neural networks, basic model of Artificial neural networks, Important terminology of ANNs, McCulloch-pitts neuron model, Linear separability, Hebb Network Supervised Learning Network: Perceptron networks, adaptive linear neuron (Adaline), Multiple adaptive linear neuron, Back propagation network, Radial basis Function network (Architecture& Training algorithms)

UNIT-II

Associative Memory Networks: Training algorithm for pattern Association, Associative memory network, Hetroassociative memory network (Architecture& Training algorithm), Bidirectional associative memory network Architecture, Discrete Bidirectional associative memory network, Continuous BAM ,Analysis of hamming distance, Energy function and storage capacity, Hopfield networks discrete &continuous. Unsupervised Learning Networks: Fixed weight competitive Nets, Kohonen self organizing network, Learning vector quantization (Architecture& Training algorithm) Adaptive Resonance theory network. Special networks: Simulated Annealing Networks, Boltzmann machine, Gaussian machine

UNIT-III

Fuzzy Logic: Introduction to Classical sets and fuzzy sets, Classical sets, Fuzzy sets: Operations and Properties. Fuzzy Relations: Cardinality,

Operations and Properties, Equivalence & tolerance. Membership function: Fuzzification, membership value assignment: Inference, rank ordering, angular fuzzy sets

UNIT-IV

Defuzzification: Lamda Cuts for fuzzy sets and relations, defuzzification methods Fuzzy arithmetic and fuzzy measures: Fuzzy arithmetic, extension principle, fuzzy measures, measures of fuzziness, fuzzy integral Fuzzy rule base and approximate reasoning: truth values and tables in fuzzy logic, fuzzy propositions formation of rules ,decomposition of compound rules, aggregation of fuzzy rules, fuzzy reasoning, fuzzy inference system, fuzzy expert systems

UNIT-V

Fuzzy decision making: Individual, multiperson, multi objective, multi attribute, Fuzzy Bayesian decision making, Fuzzy logic control system: control system design, architecture &operation of FLC system, FLC system models, Application of FLC system. Genetic Algorithm: Introduction, basic operators& terminology, Traditional algorithm vs genetic algorithm, simple GA, general genetic algorithm, schema theorem, Classification of genetic algorithm, Holland classifier systems, genetic programming , applications of genetic algorithm

Suggested Reading:

1. S. N. Sivanandam & S.N.Deepa, "Principles of Soft Computing", Wiley India, 2008.
2. Limin Fu, "Neural Networks in Computer Intelligence", McGraw Hill, 1995.
3. Timoty J. Ross, "Fuzzy Logic with Engineering Applications", McGraw Hill, 1997.

BIT 457

HUMAN COMPUTER INTERACTION
(Elective - V)

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

UNIT-I

Importance of the user interface-definition, importance of good design, brief history. Characteristics of graphical & web user interfaces-GUI, WUI, principles of interface design.

User interface design process. Knowing the client-understanding how people interact, important human characteristics, human considerations. Principals of good screen design-human considerations in screen design. Develop System menus & Navigation schemes-structures, functions, content, formatting, phrasing, choices and graphical menus.

UNIT-II

Select the proper Kinds of Windows-characteristics, components, presentation styles, types, management, organizing functions, operations. Device based controls-characteristics, selection. Screen based controls-operable, text entry/read-only, selection, combination entry/selection, and other operable controls, presentation controls, selection of proper controls. Write clear Text & Messages.

UNIT-III

Provide effective Feedback and guidance & Assistance. Provide effective Internationalization and Accessibility. Create meaningful Graphics, icons and images. Choose the proper Colors. Organize and Layout windows and pages.

UNIT-IV

Interaction Design-Introduction, goals, Conceptualizing usability. Conceptualization of interaction-Problem space, Conceptual models,

interface metaphors, interaction paradigms. Understand users-Cognition, conceptual frameworks for cognition. Collaboration and communication-Social mechanisms, Conceptual frameworks.

UNIT-V

Understanding how interfaces affect users- affective aspects, expressive interfaces, user frustration, agents. Process of interaction design-activities, characteristics, practical issues, Life cycle models. Design, Prototyping and Construction- prototyping, conceptual design, Physical design. Introducing evaluation- evaluation, frameworks. Testing and modeling users

Suggested Reading:

1. Wilbert O. Galitz , "The Essential Guide to User Interfce Design", Wiley Dreamtech, 2002.
2. Sharp, Rogers, Preece, "Interaction Design", 2nd Edition, John Wiley, 2008.

Reference:

1. John M. Caroli , "Human - Computer Interaction – In the New Millennium", Pearson Education, 2007.

BIT 458

SOFTWARE PROJECT MANAGEMENT
(Elective - V)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT – I

Introduction to Software Project Management, Stepwise: An Overview of Project Planning, Programmer Management and Project Evaluation

UNIT – II

Selection of an Appropriate Project Approach, Software Effort Estimation, Activity Planning

UNIT – III

Risk Management, Resource Allocation, Monitoring and Control

UNIT –IV

Managing Contracts, Managing People and Organizing Teams, Software Quality

UNIT – V

Small Projects, Prince2, BS 6079:1996

Suggested Reading:

1. Bob Hughes and Mike Cotterell – Software Project Management, 4th Edition – Tata McGraw Hill – 2006.

Reference:

1. Walker Royce, Software Project Management: A Unified Framework, Pearson Education – 1998.
2. Pankaj Jalote, Software Project Management, Pearson Education – 2002.

WITH EFFECT FROM THE ACADEMIC YEAR 2009-2010

BIT 459

ENTREPRENEURSHIP
(Elective - V)

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

UNIT–I

Indian Industrial Environmental – Competence, Opportunities and Challenge. Entrepreneurship and Economic growth. Small Scale Industry in India, Objectives, Linkage among small, medium and heavy industries, Types and forms of enterprises.

UNIT–II

Identification and characteristics of entrepreneurs. Emergence of First generation entrepreneurs, environmental influence and women entrepreneurs. Conception and evaluation of ideas and their sources. Coice of Technology – Collaborative interaction for Technology development.

UNIT–III

Project formulation, Analysis of market demand, Finar cial and profitability analysis and technical analysis. Project financing in India.

UNIT–IV

Project Management during construction phase, project organization, project planning and control using CPM, PERT techniques. Human aspects of project management. Assessment of tax burden.

UNIT–V

Behavioral aspects of entrepreneurs : Personality – determinants, attributes and models. Leadership concept and models. Values and attitudes. Motivation aspects. Change behavior. Time Management : Various approaches of time management, their strengths and weakness. The urgency addition and time management matrix.

Suggested Reading :

1. Vasant Desai, Dynamics of Entrepreneurial Development and Management ", Himalayas Publishing House,1997.
2. Jprasanna Chandra, "Project – Planning, Analysis Selection, Implementation and Review ", Tata McGraw Hill Publishing Co.Ltd, 1995.
3. Stephen R. Covery and Roger Merrill A., " First Things First", Simon and Scheuster publication, 1994.
4. Sudha G.S, " Organizational Behavior", National Publishing House,1996.

BIT 481

EMBEDDED SYSTEMS LAB

Instruction	3 Periods per week
Duration of University Examination	3 Hours
University Examination	50 Marks
Sessional	25 Marks

A Use of 8-bit and 32-bit Microcontrollers, (such as 8051 Microcontroller, ARM2148 / ARM2378, LPC 2141/42/44/46/48) Microcontroller and C compiler (Keil, Ride etc.) to:

1. Interface Input-Output and other units such as: Relays, LEDs, LCDs, Switches, Keypads, Stepper Motors, Sensors, ADCs, Timers
2. Demonstrate Communications: RS232, IIC and CAN protocols
3. Develop Control Applications such as: Temperature Controller, Elevator Controller,
   Traffic Controller

B. Development of Embedded Application using FPGAs, CPLDs, VHDL and Xilinx Programmable Logic Design Tools:

1. Four bit ALU
2. Pseudo Random Number Generator

C. Development and Porting of Real Time Applications on to Target machines such as Intel or other Computers using any RTOS

I. Understanding Real Time Concepts using any RTOS through Demonstration of:

1. Timing
2. Multi-Tasking
3. Semaphores
4. Message Queues
5. Round-Robin Task Scheduling
6. Preemptive Priority based Task Scheduling
7. Priority Inversion
8. Signals
9. Interrupt Service Routines

II. Application Development using any RTOS:

1. Any RTOS Booting
2. Application Development under any RTOS

BIT 482

SEMINAR

Instruction	3 Periods per week
Sessional	25 Marks

Oral presentation is an important aspect of engineering education. The objective of the seminar is to prepare the students for a systematic and independent study of the state of the art topics in a broad area of his / her specialization. Seminar topics need to be chosen by the students with advice and approval from the faculty members. Students are to be exposed to the following aspects of a seminar presentation.

- Literature Survey
- Technical writing
- Organization of the material
- Preparation of Power Point Slides
- Power Point Slide Presentation

For award of Sessional marks, students are judged, on the basis of oral and written presentation skills as well as their involvement in the discussions, by a team comprising of at least two faculty members.

Each student is required to:

a) submit a one-page synopsis to get the approval of the topic.

b) submit Seminar Report on the approved topic at least one week ahead of the scheduled day of presentation and the report should be as per the common guidelines provided by the department along with a list of references and the set of ppt slides prepared for the presentation.

c) present seminar on approved topic for about 20 minutes using ppt slides, followed by 10 minutes discussion.

d) be present on all the days of seminar presentation and to involve actively in the technical discussions/ interactions at the end of every presentation.

Seminars are to be scheduled from the 4th week of the semester to the last week of the semester and any change in the schedule is discouraged.

BIT 483

MAIN PROJECT

Instruction	6	Periods per week
Duration of University Examination		Viva
University Examination		Grade*
Sessional	50	Marks

"Solving a real life problem" should be the focus of U.G Project. Faculty members should prepare project briefs(scope and references) well in advance. They should be made available to the students at the departmental library. A project may be classified as hardware/software/ modeling/simulation. It should involve elements of techniques such as analysis, design, synthesis, etc.

The department will appoint a Project Coordinator who will be in charge of the following:

- Grouping of students (a maximum of three in a group)
- Allotment of projects and project guides
- Project monitoring at regular intervals.

All Projects allotment will be completed by the 4th week of I Semester of Final Year so that students get sufficient time for completion of their projects. Students are expected to complete Problem Definition, Literature Survey, Requirements Analysis and Design/ Methodology/ Algorithm Development, in I semester and Coding/ Implementation/ Experimentation, testing/ Results Analysis and Project Report Preparation, etc., in II Semester of the Final Year.

All the projects are to be monitoring at least twice in a semester through students presentations by a committee comprising of Project Coordinator, Supervisor and Faculty Members.

Common Guide lines for final documentation of the project report are to be provided by the department.

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* Grade: Excellent/Very Good/Good/Satisfactory/Unsatisfactory

Note: Three periods of contact load will be assigned to each project guide.